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MARCH 1982

DEVELOPMENT, FABRICATION, AND TESTING OF M36E1 FUZE SETTER

Prepared by

Anthony R. Kolanjian and Richard H. Titcomb
FAIRCHILD WESTON SYSTEMS INC.
300 ROBBINS LANE
SYOSSET, NEW YORK 11791

Under contract
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U.S. Army Electronics Research
and Development Command
Harry Diamond Laboratories
Adelphi, MD 20783

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This report describes the program undertaken for the development, assembly, and testing of the M36E1 fuze setter. The program culminated in the fabrication, test, and delivery of 10 prototype units that are designed to set the M587/M724 electronic time fuzes from 0.2 to 199.9 s in 0.1 s increments. Setting is accomplished in less than 1 s with function mode and desired time selected by means of decimal pushbutton switches on the fuze

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setter. A readout display indicates the set time. The fuze setter is battery powered and requires no field maintenance except changing of the battery. Design features incorporated in the fuze setter include self-checking capability, indication of low battery voltage, and the capability of interrogating a fuze to determine its time setting. The circuit configuration employs microprocessor components, available off the shelf, which minimize power consumption. Packaging of the fuze setter allows hand-held operation and permits functioning in an artillery ground environment. System tests demonstrate that the system complies with the specific technical requirements, while withstanding selected environmental conditions.

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1. INTRODUCTION

This report describes the development, assembly, and testing of the M36E1 fuze setter. The program described herein involved an effort, comprising several phases which were conducted between 19 June 1979 and 31 September 1981. It was conducted by the Armament Systems Department of Fairchild Weston Systems, Inc., a division of Schlumberger, for Harry Diamond Laboratories (HDL) Contract No. DAAK21-79-C-0102.

This report includes a detailed description of the fuze setter and its operation, a theoretical description of the system, timing charts, and logic diagrams.

1.1 Design Description

The M36E1 fuze setter is designed to set the M587/M724 fuze to the desired function time. Both fuzes are basically identical and are classified as electronic time fuzes. The M587 fuze is intended for artillery application including rocket-assisted projectiles, whereas the M724 fuze is intended for non-detonating cargo-type projectiles. Both fuzes are settable from 0.2 to 199.9 s in 0.1 s increments. The M587 fuze can also be set for point detonation. Setting takes less than 1 s with the M36E1 fuze setter. The mode of function and the desired function time are selected by means of pushbutton rotary switches on the fuze setter. The switches have a digital readout that can be illuminated to permit night operations. The fuze is set by inserting the nose of the fuze into a guide, provided on the setter, until contact is made. Electrical interconnections are accomplished by means of five sets of spring-loaded pins at the base of the setter guide and three concentric rings, configured as a bullseye target, on the nose of the fuze. During the setting operation, 95 percent of the fuze circuits are tested, the fuze oscillator is calibrated, and the actual time set into the fuze is verified. Light-emitting diode integrated circuits (IC's) in the setter display the set time. The fuze setter is battery powered and requires no field maintenance except replacing of the batteries. Other design features are also incorporated in the setter. These include indication of low battery voltage, the capability of interrogating a fuze to determine its time setting, and self-checking test features. Proper operation of the setter can also be checked in the field without any test equipment other than a fuze that is known to be functioning properly.

1.2 Program Background

HDL designed and developed the electronic time fuze and its associated fuze setter, in response to a Qualitative Material Requirement. The first fuze developed for this requirement, designated the M587, employed magnetic cores as the memory, since these devices do not require power after setting. In 1968, the advent of metal nitride oxide silicon (MNOS) IC technology, which can provide memory without power, led to a redesign of the fuze, because it had been determined that the use of these circuits would reduce the cost of the production fuze. The new fuze was assigned the nomenclature Fuze, Electronic Time: M587.

The M361E1 was brought through various stages to reach final design goals. The first design stage required the assembly of two breadboards, which had a CMOS microprocessor and a 2k NMOS erasable programmable read only memory (EPROM). These two breadboards also could use 1k CMOS ROM. These breadboards were used to test each configuration using improved software for both versions of the M36E1 fuze setter.

2. PROGRAM OBJECTIVES

The objective of this program was to satisfy all of the necessary technical requirements involved in the development and testing of the M36E1 fuze setter. This included a design review and preparation of a technical data package for use in the production of units to be used in the field. The basic tasks to be accomplished were as follows.

2.1 Production Engineering Improvements

(a) Decrease size and weight for ease of use.

(b) Improve safety and reliability by decreasing the number of components.

(c) Increase the number of settings from each battery under field conditions.

(d) Improve maintainability by using different assembly techniques.

2.2 Engineering Test Evaluation

(a) Fabricate two fuze setter breadboards and subject them to low and high temperature.

(b) Fabricate three fuze setters and subject them to the following environmental tests:

(1) Low temperature
(2) High temperature
(3) Electromagnetic interference (EMI)
(4) Immersion
(5) Dust/sand
(6) Drop
(7) Transportation vibration
(8) Temperature humidity
(9) Salt fog

(c) Upon completion of environmental testing of the three fuze setters above, fabricate 10 fuze setters, incorporating any modifications deemed necessary as a result of those tests, and subject them to similar environmental tests.

3. WORK ACCOMPLISHED

3.1 General

The program began in July 1979. Initial efforts were directed at program organization and the assignment of task responsibilities. Most of the personnel assigned to the program were already familiar with the project and had been associated with the previous effort for HDL under Contract No. DAAG39-76-C-0020.

A program plan which consisted of several phases was generated. These phases included design and production engineering improvements to reduce costs of both piece parts and assembly time, the incorporation of these modifications onto associated drawings, the purchase of parts required for hardware to be fabricated, the generation of specifications and test procedures, the fabrication of two breadboards and two lots of fuze setters, and the subjection of these fuze setters to functional and environmental tests.

Additional tasks were also performed in accordance with two modifications to the original contract. The first modification called for various design improvements to be completed. Included was a full data package on all phases of the software used on the

fuze setter. Some testing and modification of test equipment were also required. The second modification to the contract required design changes which appeared necessary after the test program. These changes included modifications of the battery compartment, the display circuit, the battery low circuit, and the carrying lanyard.

3.2 Production Engineering Improvements

Product improvements were generally a direct result of test results. The first change concerned the placement of the D cells in the battery compartment. The cells tended to move out of place. Relocating the contact pins solved this problem.

The next change concerned the battery cable plug. Because of stress on the wire in the cable, when the plug was removed, the cable shorted. Redesigning the plug to hold the wire more securely solved this problem.

A modification of the lanyard stud was required to solve a problem which involved the bending of the lanyard clip. By creating a larger attachment point to the housing, a larger and stronger clip could be used.

Two changes were required in the circuitry. The first change, in the battery monitoring circuit, was a different sensing zener diode selected to make full use of the battery. The second change was in the display circuit. The display would occasionally illuminate when the fuze setter was turned on. A circuit which keeps power off the display drivers until a short time after unit turn-on solved this problem.

3.3 Test Program

Three different environmental programs were run on the fuze setters. The units were divided into three groups: the first group of breadboard numbers 1004 and 1005; the second group of units 1001, 1002, and 1003; and lastly, units 1006 through 1015. All units were subjected to both high and low temperature. Some were subjected to other tests including leakage, dust, humidity, EMI, vibration, and shock. A summary of these tests is given in table 1 and figure 1.

The detail requirements of the tests are given in the military specification for the fuze setter.[1]

[1]Military Specification for Fuze Setter, M36E1, Harry Diamond Laboratories HD(P)-F-00019 (May 1980).

TABLE 1. PRODUCTION SPECIFICATION ELECTRICAL TESTS

Test No.	Test	Setting switches	Display readout	Notes/reference paragraph
1.1	Set time	188.8	188.8	3.3.1.1
1.2	Interrogate*	?	188.74 to 188.88	3.3.1.2
1.3	Set time	099.9	99.0	3.3.1.1
1.4	Set time	100.0	100.0	3.3.1.1
1.5	Set time	011.1	11.1	3.3.1.1
1.6	Set time	122.2	122.2	3.3.1.1
1.7	Set time	033.3	33.3	3.3.1.1
1.8	Set time	144.4	144.4	3.3.1.1
1.9	Set time	055.5	55.5	3.3.1.1
1.10	Set time	166.6	166.6	3.3.1.1
1.11	Set time	077.7	77.7	3.3.1.1
1.12	Set time	000.0	E†	3.3.1.1
1.13	Interrogate*	?	P‡	3.3.1.2
1.14	Set time	000.1	E	3.3.1.1
1.15	Interrogate*	?	P	3.3.1.2
1.16	Set time	000.2	0.2	3.3.1.1
1.17	Interrogate*	?	0.14 to 0.28	3.3.1.2
1.18	Set time	199.9	199.9	3.3.1.1
1.19	Interrogate*	?	199.84 to 199.98	3.3.1.2
1.20	PD mode*	PD	P	3.3.1.3
1.21	Interrogate*	?	P	3.3.1.2
1.22	Set time	188.8	188.8	Connect 3.0k ±5% between MON/Vx 3.3.3.3
1.23	Set time	188.8	188.8	Connect 3.0k ±5% between MON/GND 3.3.3.3
1.24	Set time	188.8	188.8	Connect 3.0k ±5% between MON/Vx and MON/GND 3.3.3.3

TABLE 1. PRODUCTION SPECIFICATION ELECTRICAL TESTS (Cont'd)

Test No.	Test	Setting switches	Display readout	Notes/reference paragraph
1.25	Set time	188.8	LE§	Short Circuit, MON/Vx/GD 3.3.3.3
1.26	Set time	188.8	188.8	3.3.1.1
1.27	Set time	005.6	5.6	3.3.1.1
1.28	Interrogate	?	5.54 to 5.68	3.3.1.2
1.29	Function time	-	-	Test as indicated in figure 2. Function time shall be interrogate time ±0.02
1.30	Oscillator square wave at:			
	91 s	001.5	1.5	3.3.3.6
	65 s	001.5	E	3.3.3.6
	110 s	001.5	1.5	3.3.3.6
	140 s	001.5	E	3.3.3.6
1.31	Arming signal	188.8	E	3.3.3.7
1.32	Fire signal	188.8	E	3.3.3.8

TABLE 1. PRODUCTION SPECIFICATION ELECTRICAL TESTS (Cont'd)

Test No.	Test	Minimum	Maximum	Unit	Reference paragraph
1.33	Time base freq.	2457.477	2457.723	kHz	3.3.3.2
1.34	Set to 1.5 and verify set. Measure +Vp at:				
	ambient temp	28.0	30.0	V	3.3.3.4
	+63°C	28.5	32.0	V	3.3.3.4
	-40°C	26.0	28.5	V	3.3.3.4
1.35	Measure -Vp at:				
	ambient temp	-28.0	-30.0	V	3.3.3.4
	+63°C	-28.0	-32.0	V	3.3.3.4
	-40°C	-26.0	-28.5	V	3.3.3.4
1.36	Measure -Vx at:				
	ambient temp	-25.0	-26.8	V	3.3.3.4
	+63°C	-26.0	-28.0	V	3.3.3.4
	-40°C	-22.5	-25.0	V	3.3.3.4
1.37	Calculate (-Vp)-(-Vx) at:				
	ambient temp	-2.5	-	V	3.3.3.4
	+63°C	-2.5	-	V	3.3.3.4
	-40°C	-2.5	-	V	3.3.3.4
1.38	Measure duration of +Vp at:				
	ambient temp	50.2	50.4	ms	3.3.3.5
	+63°C	50.2	50.4	ms	3.3.3.5
	-40°C	50.2	50.4	ms	3.3.3.5
1.39	Measure duration of -VP at:				
	ambient temp	50.2	50.4	ms	3.3.3.5
	+63°C	50.2	50.4	ms	3.3.3.5
	-40°C	50.2	50.4	ms	3.3.3.5

TABLE 1. PRODUCTION SPECIFICATION ELECTRICAL TESTS (Cont'd)

Test No.	Test	Minimum	Maximum	Unit	Reference paragraph
1.40	Max. low-battery voltage when setting 188.8 at				
	ambient temp	5.4	5.6	V	3.3.4.4
	+63°C	5.6	5.9	V	3.3.4.4
	-40°C	5.0	5.3	V	3.3.4.4
1.41	(Measure test 1.40)-(max low battery voltage without setting a fuze) at:				
	ambient temp	0.3	0.5	V	3.3.4.4
	+63°C	0.5	0.7	V	3.3.4.4
	-40°C	0.2	0.4	V	3.3.4.4
1.42	Turn-on time	125	225	ms	3.3.4.1
1.43	Turn-off time	250	450	ms	3.3.4.2
1.44	Display time	4.0	6.0	s	3.3.4.3
1.45	Setting current	-	450	mA	3.3.4.5
1.46	Display current	-	200	mA	3.3.4.6
1.47	Turn-off current	-	75	mA	3.3.4.7
1.48	Standby current	-	1.0	A	3.3.4.8

*The time setting switches can be in any position during interrogate.
†E indicates improper operation of the fuze or fuze setter.
‡P indicates a point detonation mode of operation.
§LE indicates improper operation of the fuze or fuze setter as well as a low battery voltage.

PRODUCTION SPECIFICATION TEST DISTRIBUTION

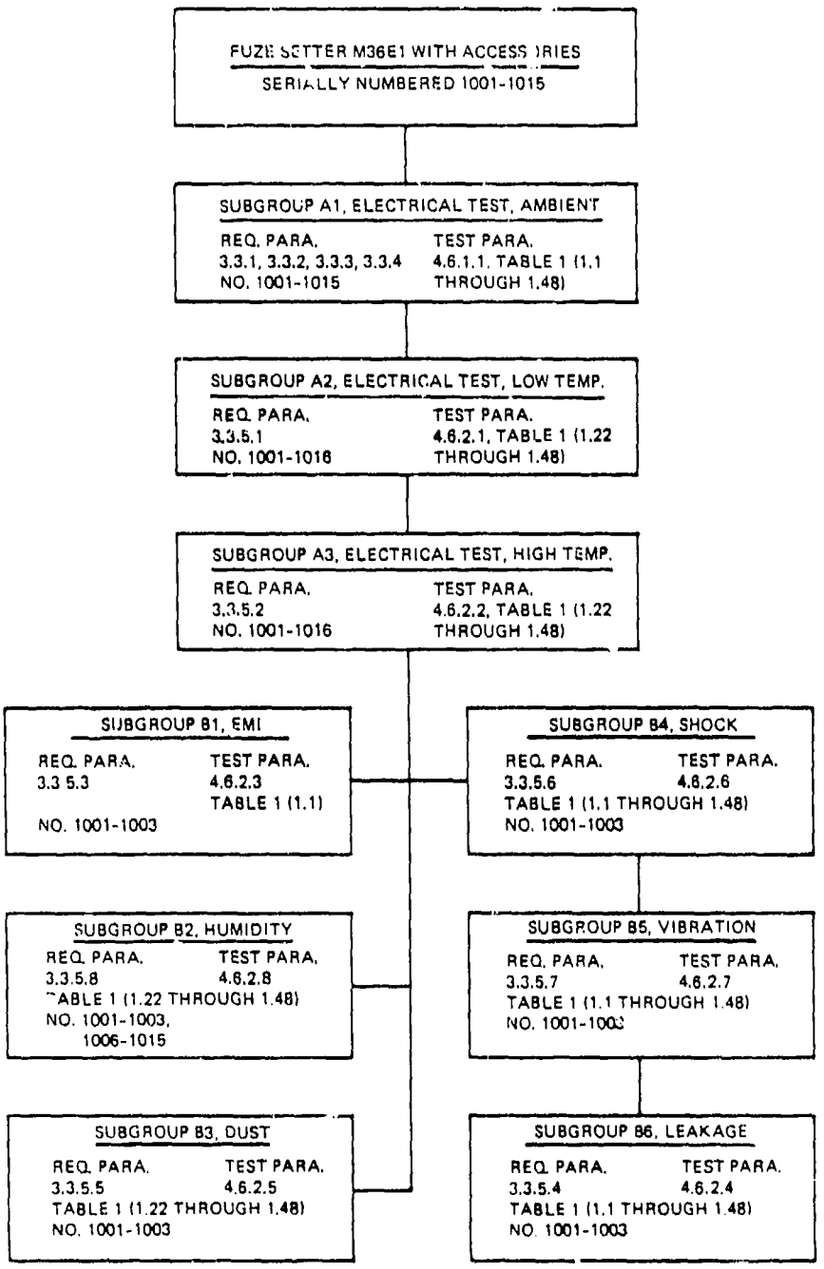

Figure 1. FAAS and lot sample flow chart.

During the environmental testing on units 1001 to 1003, various failures occurred. During the temperature testing, two incorrect components were found which caused the units to fail. These were changed and the unit tests continued. During immersion testing a leakage problem was found with the lamps in the setting switches. This problem was overcome by proper tightening of the lamps. The first three units also used excessive power. This was caused by the use of an NMOS memory IC. This memory IC was changed to a CMOS device on all later units. This greatly reduced power consumption.

Procedures and test distribution are given in each lot summary report for DT/OT-II units. A summary of the test distribution is shown in figures 2 and 3.

After the completion of testing at Fairchild's facility on units 1006 through 1015, they were turned over to HDL. HDL then dispersed these units to various locations for testing. Six units were sent to the Yuma Proving Grounds for extensive environmental and functional tests. These tests are summarized in the test outline shown in figure 2. The purpose of these tests is to provide data from which the accuracy, battery life, and safety of the fuze setter can be determined. Tests done include temperature (-40°F, +70°F, and +145°F), temperature shock, secured cargo, loose cargo, 4 ft drop, center impact, sand/dust, immersion, and salt/fog. Battery testing was also carried out in an attempt to ascertain the number of sets attainable from each type of battery. All testing except for the battery, salt/fog, and sand/dust tests were done at the Yuma Proving Grounds. These tests were performed at the Fairchild facility in Syosset, New York. All tests were performed according to the Detailed Test Plan for Development Test II on M36E1 Fuze Setter[2] dated June 1980.

In addition to the development testing done at Yuma, an operational test program was conducted at Ft. Sill, Oklahoma. The purpose of this test program was to determine the suitability of the fuze setter in actual field application. Test areas include physical and design characteristics, battery firing, operation and human factors, training, transportability, reliability, availability, and maintainability. All testing was performed according to Operational Test II of the Electronic Time Fuze Setter M36E1[3] dated 29 May 1980.

[2]Detailed Test Plan Development Test II of M36E1 Fuze Setter for M587/M724 Fuze, Electronic Time, John D. Kruger, US Army Yuma Proving Ground (June 1980).

[3]Operational Test II of the Electronic Time Fuze Setter M36E1, Major Gerard G. James, US Army Field Artillery Board (29 May 1980).

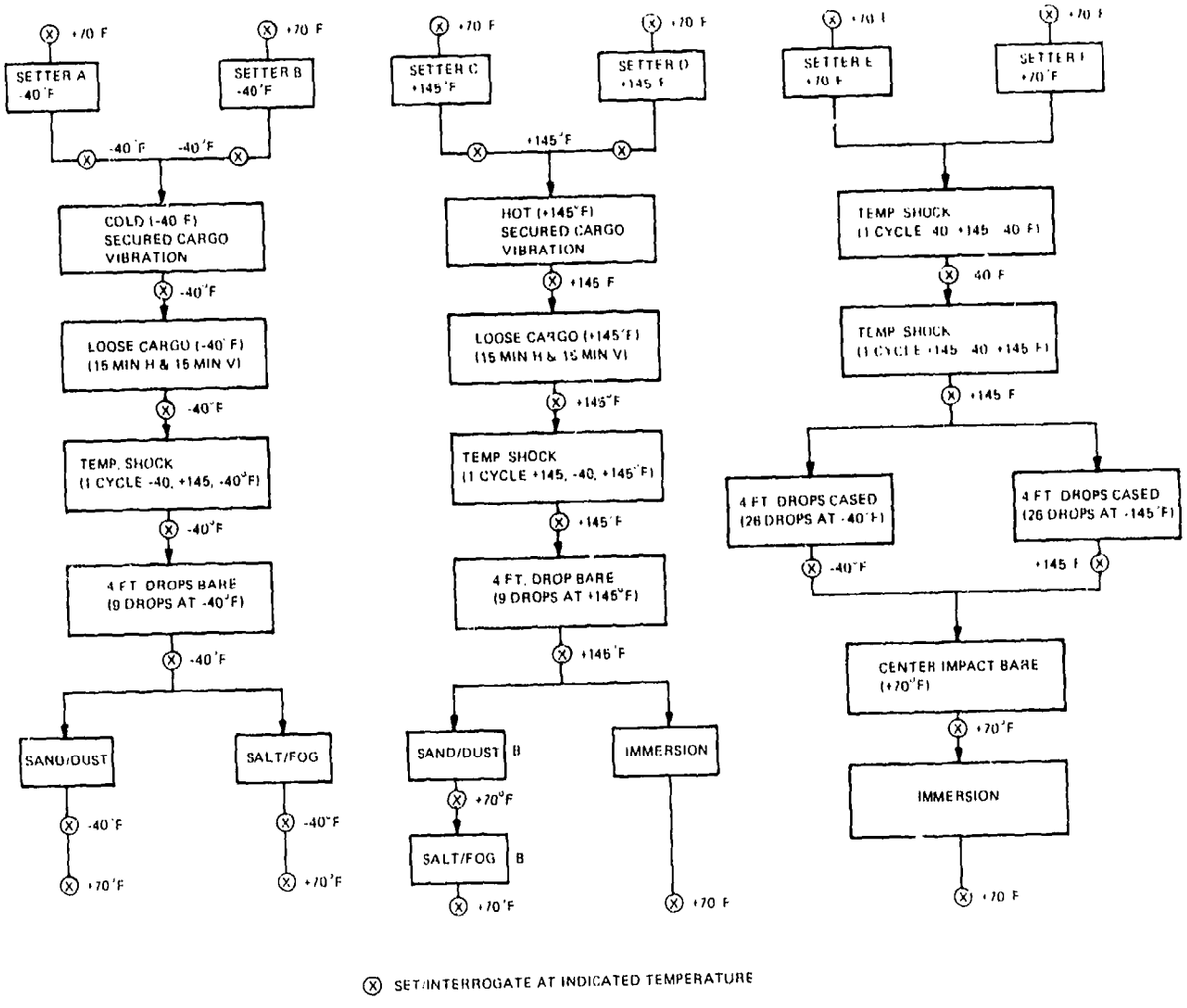

Figure 2. Rough handling and environmental subtest outline for DT-II testing.

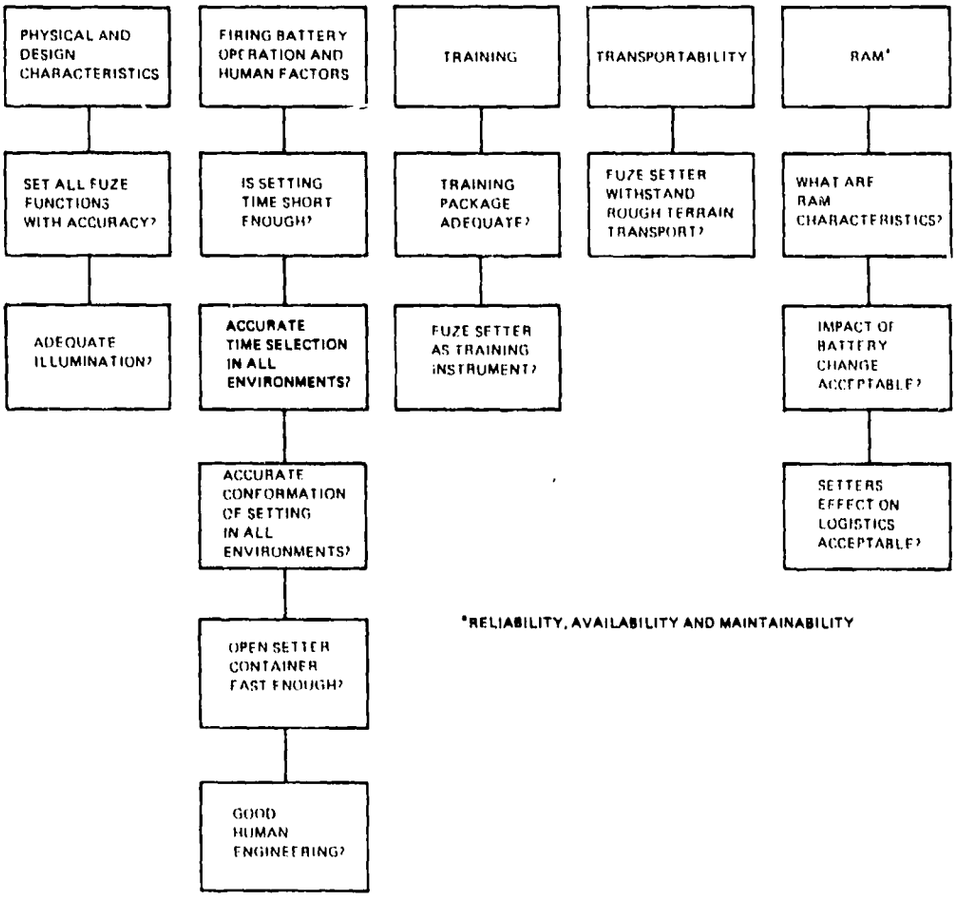

Figure 3. OT-II test objectives.

During the DT-II testing two problems were discovered. One was the recurrence of the leakage problem in the setting switch lamps, caused by improper tightening of the lamps. The second problem was traced to an intermittent crystal. The crystal apparently broke during a shock test but did not show up as a failure on a test until it was shipped to the Fairchild facility in Syosset. Replacing the crystal solved the problem.

During OT-II testing problems were found with the carrying lanyard and the battery cable. The lanyard clip tended to bend and the lanyard separated from the setter. The battery cable tended to short because an improper type of wire was used in the cable assembly.

The lanyard problem will be solved by changing the clip on all future units.

The cable problem was solved by changing the wire used and anchoring it more securely to its plug.

A software change which occurred after the OT-II, DT-II testing required a change in ROM's. The new ROM was physically identical to the previously used one; the only difference was the program carried in the ROM. The new ROM was installed in breadboard 1004 and tested at -40°F, 70°F, and +145°F. These tests were successfully completed and unit 1006 was retrofitted with the new ROM.

3.4 Packaging Features

Figures 4 through 9 illustrate various features of the package design of the M36E1 fuze setter, S/N 1006 through 1015. External views of the fuze setter are shown in figures 4 and 5. The fuze probe, setting switches, illumination switch, display readout window, and lanyard are all indicated. Some of the human engineering features of the fuze setter are apparent in these figures. The fuze setter, weighing less than 6 lb, is 6.9 in. high, 3.75 in. wide, and 4.3 in. deep. The reduction in size and weight allows the fuze setter to be held in one hand. Surfaces that will be used to hold the fuze setter have a "ribbed" surface for an improved grip.

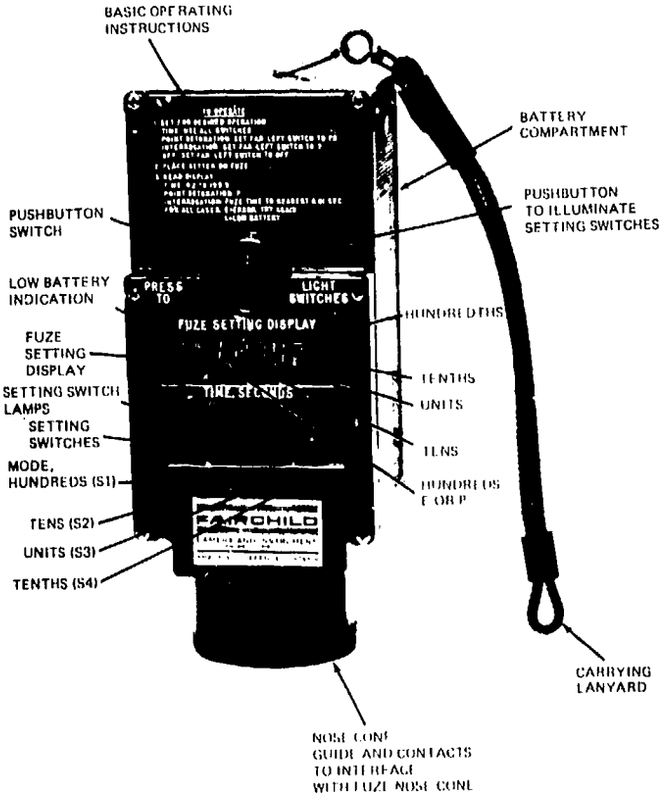

Figure 4. Controls and indicators.

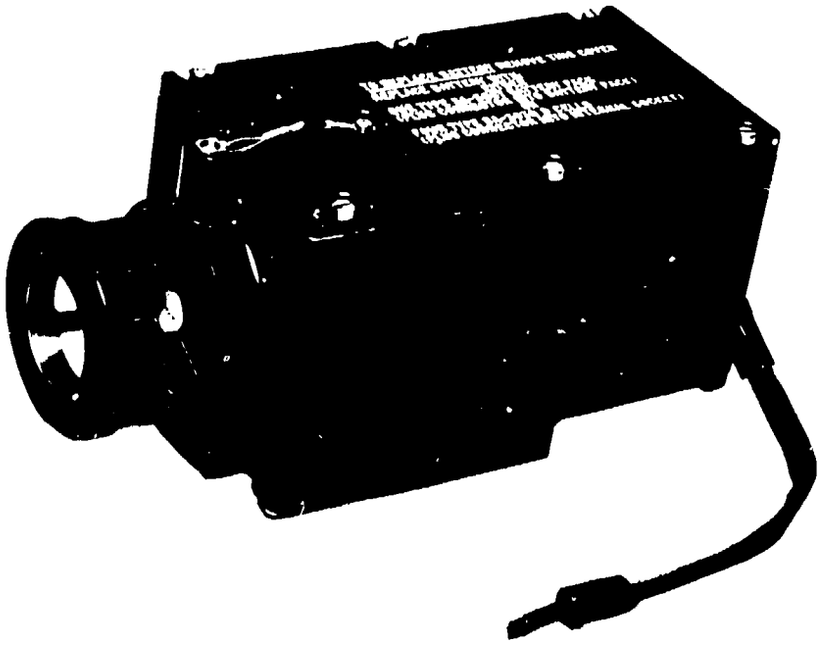

Figure 5. Fuze setter battery cover.

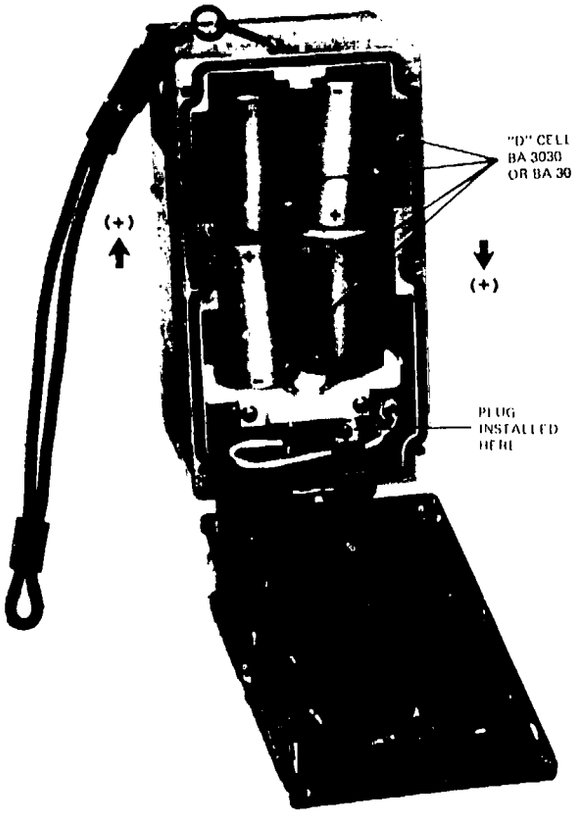

Figure 6. Battery compartment with "D"-cells installed.

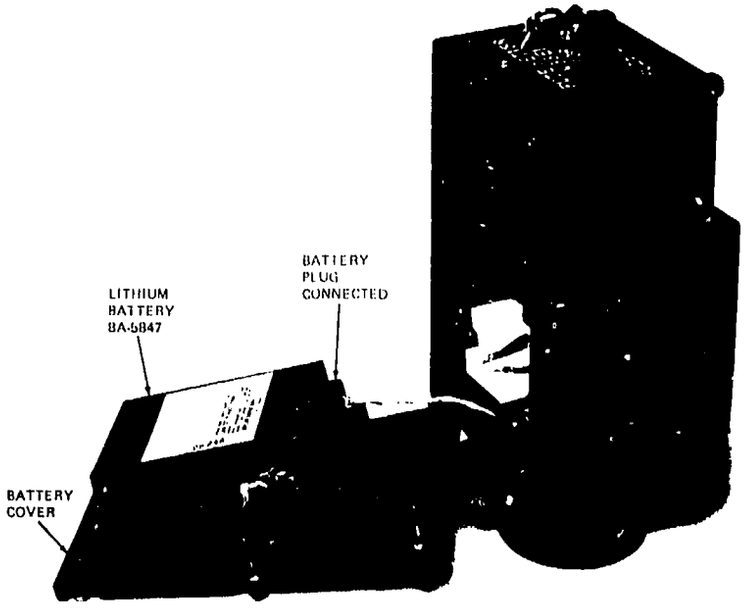

Figure 7. Battery compartment with lithium battery installed.

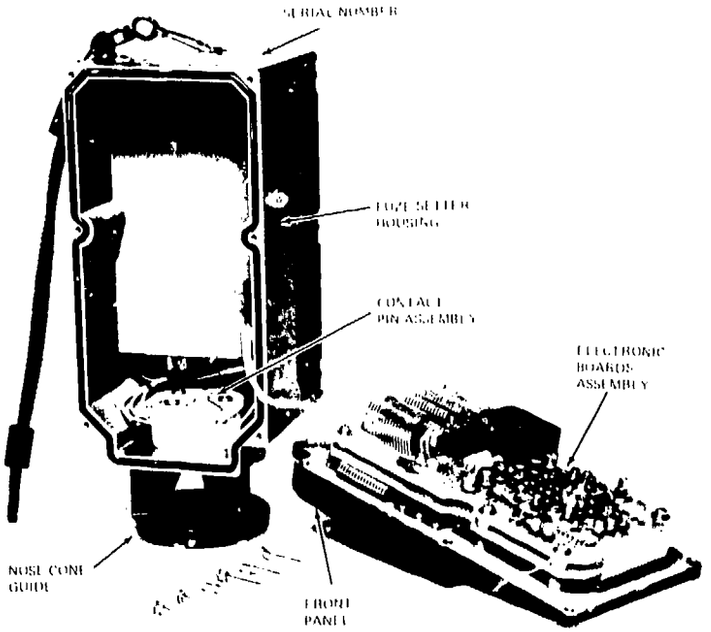

Figure 8. Front panel removed.

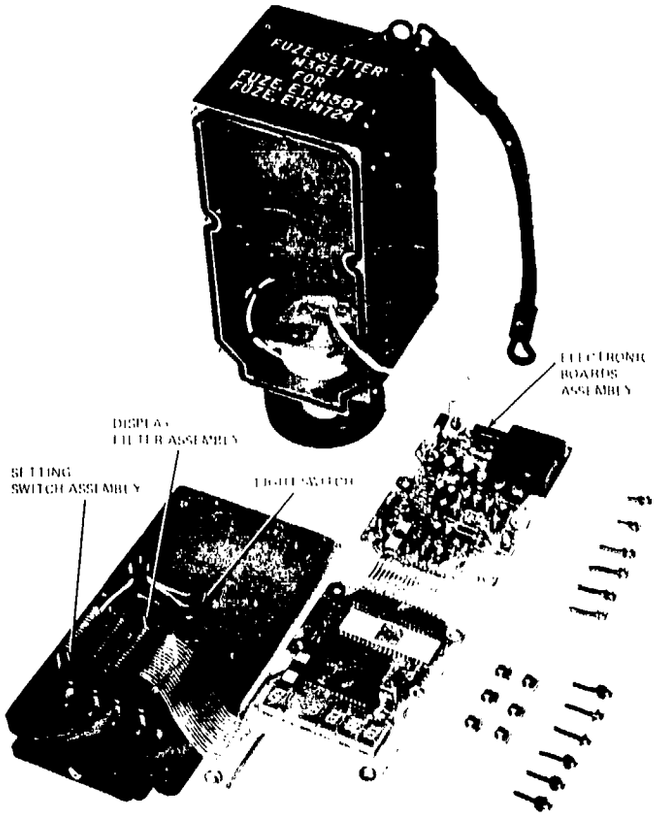

Figure 9. Electronics removed.

The setting switches are on the same surface as the display readout, to make it easier to confirm a setting. The setting switches themselves can be used easily under all conditions even by someone wearing arctic gloves. The setting switch illumination switch is located so that it can be activated with the same hand that is used to hold the fuze setter.

A lanyard is provided to carry the fuze setter. The user can wear this lanyard while setting fuzes to avoid accidentally dropping the fuze setter.

Figures 6 and 7 show the battery compartment with the two different types of batteries installed. To change a battery, six captive screws in the rear cover must be unscrewed from the housing. To prevent water of soil entering the electronics compartment while the battery is changed, the two compartments have a watertight seal between them.

Figure 8 shows the front panel assembly separated from the main fuze setter housing. To remove the front panel assembly, six screws must be removed.

Figure 9 shows the front panel assembly disassembled. To disassemble the front panel, six other screws must be removed. At this point, all the circuitry in the fuze setter is accessible for troubleshooting.

All mating surfaces and all components protruding through the outer walls of the setter are sealed with a gasket or O ring.

3.5 Reliability Analysis

A reliability analysis was performed on the design of the M36E1 fuze setter. A reliability report[4] was generated encompassing the following basic areas:

(1) A review of the reliability sensitive components and assemblies to ensure the following:

   (a) All parts were within the specified requirements of the program.

   (b) Proper application of each part type had been made.

   (c) Established reliability and JAN-TX parts had been employed to the maximum extent.

   (d) Backup qualification information from the vendor justified the employment of non-standard parts where their use was unavoidable.

(2) An analysis of the thermal conditions in all semiconductor components at the worst-case ambient temperature conditions, to ensure adequate safety during use.

[4]Reliability Analysis Report for Microprocessor Fuze Setter M36E1, Fairchild Weston Document No. ED-CP-8 Rev. B (August 1980).

(3) An analysis of the electrical stresses on all components to insure that none were being used at levels which would seriously degrade the reliability of the device. These data were further required to establish the statistical failure rate of each part.

(4) An analysis of the predicted inherent reliability of the fuze setter under field use conditions.

The thermal, electrical-stress, and failure rate analyses indicated a very conservative design. The reliability analysis indicated a mean-time-between-failures (MTBF) for the entire fuze setter of 64,000 hours at the worst-case ambient condition of +60°C. At this condition, the reliability of successively setting 1000 fuzes at the maximum rate of one every 20 s is 0.999913. At lower temperatures, this reliability would improve, up to a limiting level of approximately 0.9999 at +25°C, for the complete fuze setter. Since field usage is expected to be somewhere between these limits, there is a high level of confidence that this device will perform its mission function very reliably.

3.6 Safety Analysis

A safety prediction report[5] was prepared. The objectives were to determine the numerical probability of setting a fuze to a set time other than that which is displayed by the fuze setter. Special consideration was given to the situation where a fuze is set to an earlier time than indicated by the fuze setter. All three modes of operation were taken into account: the set-time mode, the point-detonation mode, and the interrogation mode.

The safety prediction probabilities were as follows:

Mode	Probability
Set time	3.0×10^{-9}
Point detonation	3.5×10^{-9}
Interrogate	3.0×10^{-9}

The set-time and point-detonation safety probabilities compared favorably with the general requirements, per MIL-STD-332, of 0.4×10^{-6}.

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[5]Safety Analysis for Microprocessor Fuze Setter M36E1, Fairchild Weston Document No. ED-AJ-340 (25 February 1981).

3.7 Maintenance Report

A general support manual[6] was prepared for use by operator, organizational, direct support, and general support personnel in support of M36E1 fuze setter. A repair parts list and special tool list are also included.

Data included in the manual are physical and functional descriptions and instructions for the fuze setter's use, care, and handling. A troubleshooting guide is also included.

This manual gives all the necessary information for the repair and maintenance of the fuze setter. It can be used at all levels of maintenance from field to depot.

3.8 Design Modifications

3.8.1 Probe Self-Alignment

All probe design features from the M36 fuze setter were retained in the M36E1 fuze setter. The only change in design was a modification to the length of the probe. A shorter probe still maintains all the alignment properties of a longer probe and allows for a shorter overall package.

The composite drawings of all related piece parts showing proper connection under worst-case tolerances are shown in figures 10 and 11. Figure 11 illustrates the minimum contact depression when the nose cone is at its maximum contour. Figure 11 illustrates the maximum eccentricity when the nose cone is at its minimum contour. It can be seen that under these worst-case conditions proper connection is made between the fuze setter and a fuze.

3.8.2 Preparation of Specification Control Drawings

The technical data package was reviewed for compatibility with drawing requirements. All source control drawings were converted to specification control drawings with the respective requirements for each purchased part being added to the drawing. In this manner, all purchased items in the parts list of the technical data package are identified by either a military specification number or a specification control drawing.

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[6]Operators, Organizational, Direct Support and General Support Maintenance Manual, Department of the Army, TM9-1290-363-14&P (30 November 1980).

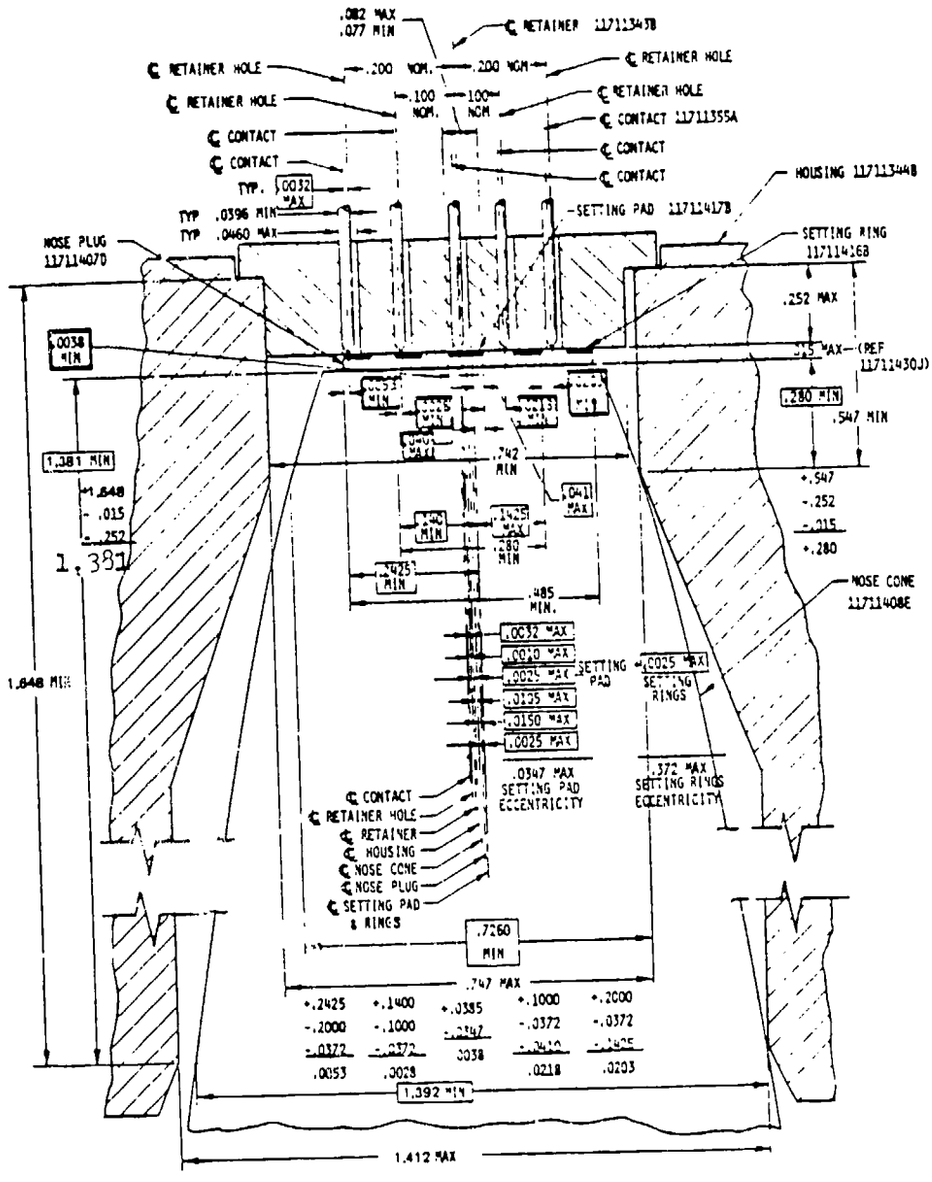


Figure 10. Maximum contact eccentricity.

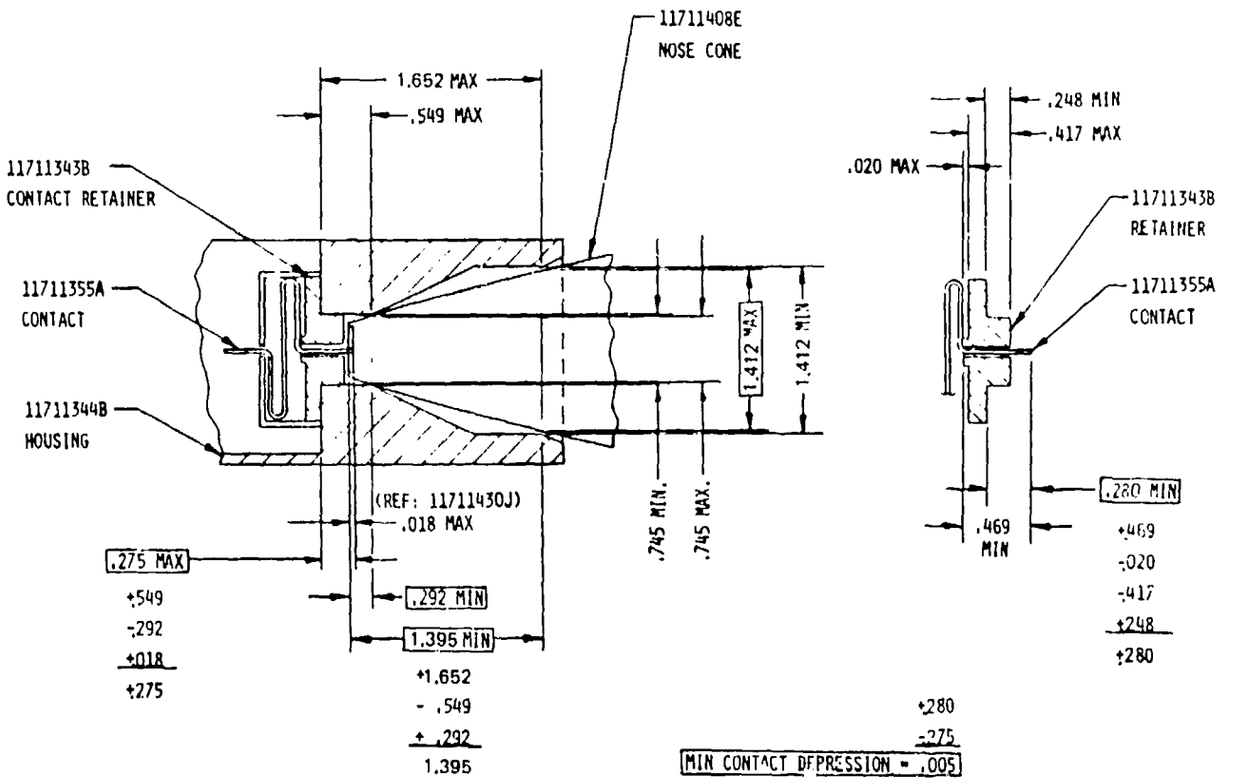


Figure 11. Minimum contact depression.

3.8.3 Battery Performance Characteristics

The performance characteristics of the various batteries to be used in the fuze setter were investigated. The batteries that can be used in the fuze setter are as follows.

(1) The BA-5847 lithium battery. This battery comes in a cardboard package which contains two 3-V lithium D-cells, a thermal fuse, and a 3-A fuse.

(2) Four BA-3030 alkaline batteries.

(3) Four BA-30 zinc-carbon batteries. The BA-30 batteries can only be used above 0°F.

The batteries were tested to determine the number of settings each type would give under different temperature conditions. Since all three types of batteries are primary batteries (nonrechargeable) their probable life in the field, under all conditions, must be well known. The testing was done by placing the fuze setter and battery in a temperature chamber and then, using an automatic cycling fuze simulator, a time was set every 4 s. The simulator registers how many settings are made. A chart recorder is also used to record the battery voltage and the output of the low-voltage circuit. Table 2 shows the results of this testing. Figure 12 shows battery life.

3.9 Drawing Lists

Through the evolution of the fuze setter from breadboard to final unit, various changes have taken place in mechanical and electrical design. Serial No. 1004 and 1005 were breadboard models and were used to prove the basic design as functional. Serial No. 1001, 1002, and 1003 were used to initiate testing and to troubleshoot problems in design under rigorous environmental conditions. Serial No. 1006 to 1015 were used for final testing and included design improvements found necessary as a result of testing on units 1001 to 1003. The drawings list for units 1006 to 1015 is shown in table 3. During test on units 1006 to 1015, further problems were found and design changes to solve these problems will be included in any future models of the fuze setter. Drawings will be revised by means of Engineering Change Proposals.

4. THEORY OF OPERATION

4.1 General

The fuze setter is designed to set the fuze to the desired function time in a setting time of 1 s. The desired function time is set on the fuze setter switches, which have a digital readout. The fuze setter is pressed onto the fuze nose cone until the display showing the set time is illuminated; the fuze is then set, and the fuze setter can be removed. If the point detonation (PD) option is chosen, the display will present a P. If the fuze cannot be set to the desired time but is still functional, the display will present an E. In either of the latter two conditions the fuze will function in the PD mode when used. The fuze setter will set the fuze in any physical position and in darkness. It requires no maintenance, except for the changing of batteries. Proper operation of the fuze setter can be checked in the field without any test equipment other than a properly working fuze.

TABLE 2. BATTERY TEST DATA

Breadboard* S/N	Battery† number	Battery type	Test temp	Number of Settings†	
				188.8	L188.8
1004	#03	Lithium BA-5847	-40°F	82190	2550
1005	#06	Lithium BA-5847	-40°F	75025	24678
1004	#09	Lithium BA-5847	-40°F	78564	13836
1004	#01	Lithium BA-5847	+70°F	75222	888
1005	#04	Lithium BA-5847	+70°F	85800	59400
1004	#07	Lithium BA-5847	+70°F	127781	8487
1004	#02	Lithium BA-5847	+145°F	82765	1027
1004	#05	Lithium BA-5847	+145°F	86901	2500
1004	#08	Lithium BA-5847	+145°F	81461	1082
1004	Package #02	Alkaline BA-3030	-40°F	990	4694
1004	Package #17	Alkaline BA-3030	-40°F	1334	3886
1004	Package #18	Alkaline BA-3030	-40°F	750	3890
1004	Package #01	Alkaline BA-3030	+70°F	37641	43981
1004	Package #15	Alkaline BA-3030	+70°F	37120	35380
1004	Package #16	Alkaline BA-3030	+70°F	35032	46052

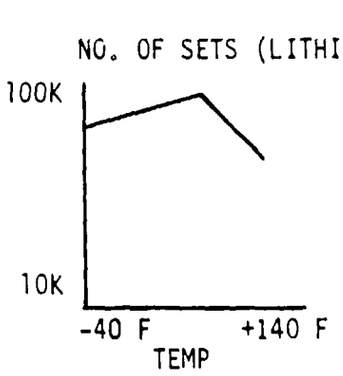
TABLE 2. BATTERY TEST DATA - (Cont'd)

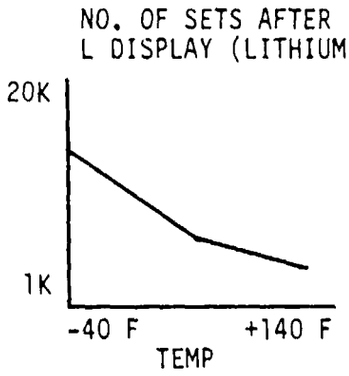
Breadboard* S/N	Battery† number	Battery type	Test temp	Number of Settings†	
				188.8	L188.8
1004	Package #05	Alkaline BA-3030	+145°F	28600	48886
1004	Package #13	Alkaline BA-3030	+145°F	396	68971
1004	Package #14	Alkaline BA-3030	+145°F	30491	39259
1004	#04	Zinc Carbon 4-(BA30)	0°F	-	2291
1004	#10	Zinc Carbon 4-(BA30)	0°F	754	7540
1004	#11	Zinc Carbon 4-(BA30)	0°F	406	7424
1004	#07	Zinc Carbon 4-(BA30)	+70°F	2958	16642
1004	#08	Zinc Carbon 4-(BA30)	+70°F	4756	17516
1004	#09	Zinc Carbon 4-(BA30)	+70°F	3132	16182
1004	#06	Zinc Carbon 4-(BA30)	+145°F	2785	29755
1004	#11	Zinc Carbon 4-(BA30)	+145°F	8000	41000
1004	#12	Zinc Carbon 4-(BA30)	+145°F	396	15322

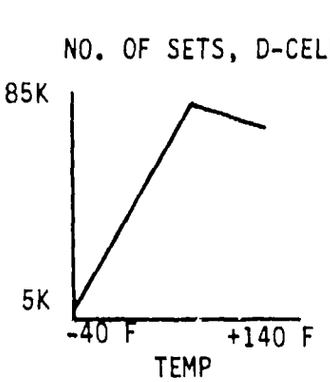
*All Breadboards use a JANTX-1N973C for the "L" sense circuit (VR1).

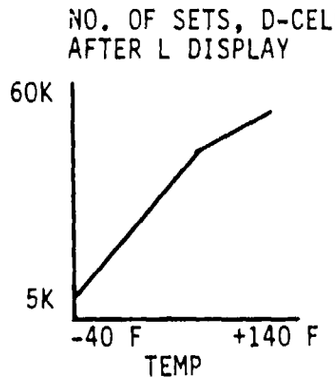
†All batteries are new and unused at beginning of test (batteries are not broken-in before test).

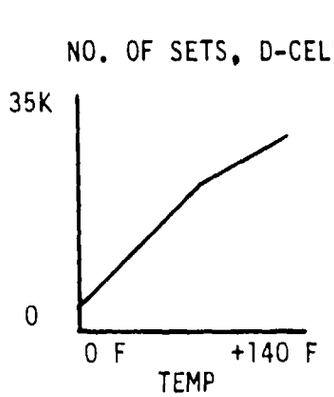
±Test ended when first "L" only was displayed.











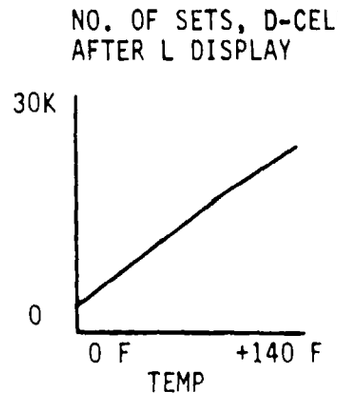


Figure 12. Temperature versus sets (BA-5847, BA-3030, BA-30) (sheet 1 of 2).

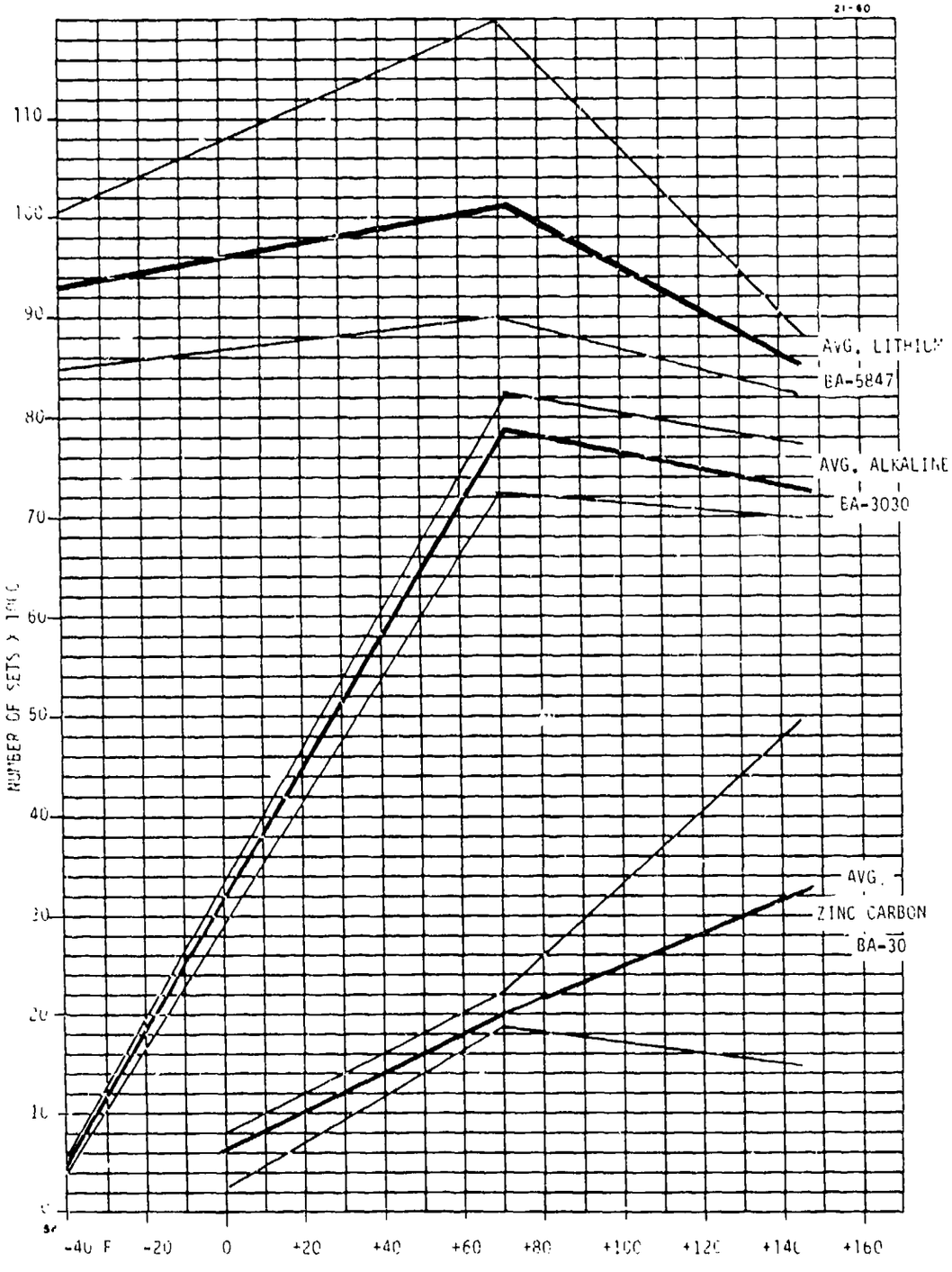


Figure 12. Temperature versus sets (BA-5847, BA-3030, BA-30 (sheet 2 of 2).

TABLE 3. FUZE SETTER: M36E1 DRAWING LIST

Drawing Number	Rev	Title
F11727050		CONTAINER, FUZE SETTER: M36E1, SHIPPING & STORAGE ASSEMBLY
F11727067		CARRYING CASE, FUZE SETTER: M36E1
F11727044		BOX, AMMUNITION, M2A1 ASSEMBLY
F11727064		PACKAGING INSERT
F11727068		COVER, INSERT
F11727000		FUZE SETTER: M36E1 ASSEMBLY
F11727004		SCHEMATIC FUZE SETTER M37E1
F11727005		HOUSING
F11727007		COVER, BATTERY
C11727026		TERMINAL, INSULATED
C11727027		CONTACT
D11727028		RETAINER, CONTACT
C11727029		COVER, CONTACT
B11717035		CUSHION, D-CELL
B11727036		CUSHION, BATTERY, UPPER
C11727037		WASHER, SADDLE
C11727042		SCREW, CAPTIVE
B11727043		STUD, LANYARD
F11727045		PRINTED WIRING MASTER, CONTACT SEAL
C11727046		PACKING, PREFORMED "O"-RING
C11727049		TERMINAL, FEEDTHROUGH
A11727053		LANYARD, FUZE SETTER
B11727051		UPPER BATTERY CONTACT ASSEMBLY
C11727024		PLATE MOUNTING (UPPER)
B11727031		CONTACT, JUMPER
C11727052		LOWER BATTERY CONTACT ASSEMBLY
D11727023		PLATE MOUNTING (LOWER)
C11727040		CONTACT, BATTERY
C11727054		BATTERY PLUG ASSEMBLY
C11727039		BLOCK, PLUG
C11727048		PIN, CONTACT, MALE
C11727056		BATTERY COVER RETAINER ASSEMBLY
B11727063		RETAINER
F11727001		FRONT PANEL ASSEMBLY
F11727006		PANEL, FRONT
C11727008		SPACER
D11727012		SWITCH, ROTARY
C11727013		GASKET, FILTER
C11727014		PLATE, FILTER
C11727015		JUMPER, PRINTED CIRCUIT BOARD
B11727025		GASKET, SWITCH
C11727038		SWITCH, PUSHBUTTON
C11727046		PACKING, PREFORMED "O"-RING
C11727011		FILTER, ANTI-REFLECTION
A11727009		LIGHT CONTROL FILM
F11727070		ELECTRONIC BOARDS ASSEMBLY
C11727015		JUMPER, PRINTED CIRCUIT BOARD
F11727002		DISPLAY & LOGIC BOARD ASSEMBLY
A11727022		DISPLAY, SEVEN-SEGMENT
A11727057		INTEGRATED CIRCUIT (1802)
A11727058		INTEGRATED CIRCUIT (1833)
A11727059		INTEGRATED CIRCUIT (4043)
A11727061		INTEGRATED CIRCUIT (4094)
A11727062		INTEGRATED CIRCUIT (7218A)
F11727065		PRINTED WIRING MASTER, DISPLAY & LOGIC
F11727003		POWER & INTERFACE BOARD ASSEMBLY
C11727037		WASHER, SADDLE
F11727066		PRINTED WIRING MASTER, POWER & INTERFACE
C11727021		TRANSFORMER ASSEMBLY
B11727018		TERMINAL
C11727017		TRANSFORMER, TOROIDAL
C11727016		CORE, MAGNETIC
C11727020		ENCAPSULATION CUP, ALTERATION
C11727019		ENCAPSULATION CUP

The fuze setter includes an interrogation switch position (?), to enable a previously set fuze to be read without disturbing its setting. The interrogation feature permits an independent verification. It also permits anyone to determine the time setting of a fuze with an unknown setting, or to check a fuze before returning it to stockpile.

The circuit is designed to operate at low-impedance levels, so that contact dirt and moisture will not affect operation. The fuze setter requires a battery of 6 V. The lithium (BA-5847) battery enables the fuze setter to operate over the temperature range of -40°F to +145°F.

4.2 Operating Sequence

The fuze is set by contacting the probe of the fuze setter and fuze nose. The probe of the fuze setter contains three sets of spring-loaded pins that make contact with the bull's-eye terminals located on the nose of the fuze. When the fuze setter is applied to the fuze, the two longer pins (ground and monitor line) make contact before the third pin (V_X or power line) makes contact. When the third pin contact is completed, the following automatic sequence occurs:

(1) Power in the fuze setter is turned on after a slight delay to eliminate the effect of any contact jitter.

(2) The fuze scalar and memory counters are checked for proper operation.

(3) The fuze counter is driven in the fast mode, which means that it is driven directly by the fuze oscillator, bypassing the scalar. Counting fuze oscillator pulses over a time interval determined by the precision clock and the dial setting in the fuze setter automatically corrects the number of counts for a deviation of the fuze oscillator from its nominal frequency.

(4) The count is stored in the fuze memory.

(5) The actual stored fuze time is verified in the fast mode against the fuze setter gating period. If the stored fuze time agrees with the desired fuze time, the display illuminates, showing the correct fuze time.

(6) When the fuze setter is removed, its power turn-off is delayed so that contact jitter will not cause the fuze setting to be disturbed.

(7) If the fuze is being set PD, a P will be displayed, and if the fuze setter or the fuze malfunctions but is still operational during the setting operation, the fuze setter will display an E. When subsequently fired, the fuze will function PD. If not fired, the fuze can be reset for the time function or fired in the PD option if the time mode is inoperative.

4.3 Other Design Features

If the fuze setter battery voltage is low, the left-most digit display will present an L when the fuze is set. The L is a reminder that the battery voltage is low and that the batteries should be changed. This indication occurs before battery voltage declines to the extent that the fuze setter will no longer function. When battery voltage is so low (less than 4.5 V) that proper operation can no longer be assured, an "L" will be displayed in the left-most digit with no other digits displayed.

The fuze setter can be used to interrogate a fuze to determine its time setting. If the mode switch is set to "?" and a nominal fuze setting operation is attempted, the time set in the fuze will show on the display. This operation is performed without any change in the fuze memory. If the fuze was in the PD condition, a P will be presented with no change in the fuze memory.

The fuze setter clock frequency is crystal controlled. Normally, this frequency will not need checking; it can be checked, however, without special test equipment. Let a fuze be set to some arbitrary long time. Then interrogate the set time with at least three fuze setters. If any fuze setter indicates a time different from the others, the clock frequency is in error, and that fuze setter should not be used to set a fuze. A test point is supplied on the display and logic board where the oscillator frequency can be monitored. This test point can only be used when the fuze setter is disassembled.

4.4. Operating Instructions

The set of operating instructions shown in Table 4 is to be employed when setting a fuze and/or verifying the correct operation of a fuze setter. This set of instructions is engraved on the front cover of the fuze setter. A more detailed set of operating instructions is given in Table 5.

TABLE 4. FRONT COVER OPERATING INSTRUCTIONS

	To Operate
1	Set for desired operation. Time: Use all switches Point Detonation: Set far-left switch to PD Interrogation: Set far-left switch to ? OFF: Set far-left switch to off
2	Place setter on Fuze
3	Read display Time: 0.2 to 199.9 Point Detonation: P Interrogation: Fuze time to nearest 0.01 s For all cases: E = Error, Try again L = Low battery

TABLE 5. DETAILED OPERATING INSTRUCTIONS

a. Illumination of setting switches.

Press pushbutton to light setting switches (except when mode switch is in OFF position).

b. Setting switch positions.

Mode	:	OFF, 0, 1, ?, PD, OFF, 0, 1, ?, PD
Time, seconds (tens)	:	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
Time, seconds (units)	:	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
Time, seconds (tenths)	:	0, 1, 2, 3, 4, 5, 6, 7, 8, 9

c. Display check (Contact properly operating fuze nose and setter probe).

Use 1 Mode, setting 188.88.	Display reads 188.8
Use PD Mode.	Display reads P.

TABLE 5. DETAILED OPERATING INSTRUCTIONS (Cont'd)

d. Choose desired mode on mode switch.

OFF: To turn fuze setter off.
0 : To set a desired time function less than 100 s.
1 : To set a desired time function greater than 100 s.
? : To interrogate a fuze without changing its setting.

PD : To set a point detonating function only.

e. If 0, 1, is chosen, enter desired time on time switches (0.2 to 199.9 s).

f. Contact fuze nose and fuze setter probe until display activates (less than 1 s).

g. Read Display

In 0, 1 Mode: Display matching dial setting indicates properly set time function.
Display of E indicates error (Try again: use new fuze if E persists).
Display will read E when trying to set 0.0 or 0.1 s.

In PD Mode: Display of P indicates properly set impact function. Display of E indicates error (Try again: use new fuze if E persists).

In ? Mode: Display will read previously set time function to nearest 0.01 s (set time +0.08 to 0.06).
Display of P indicates fuze was previously set for impact.
Display of E indicates error (Try again: use new fuze if E persists).

In all Modes: Display of L indicates low voltage (change battery at earliest opportunity).

h. Remove fuze from fuze setter when proper setting is displayed. Fire projectile.

i. Fuze setter probe contacts may be cleaned as required, using Cleaning Brush 8448462.

4.5 Battery Changing Instructions

Engraved on the rear cover of the fuze setter are instructions for changing the batteries. Within the battery compartment figures are supplied to show the proper orientation of D cell batteries. Table 6 is a listing of the instructions supplied on the rear cover of the fuze setter.

TABLE 6. REAR COVER BATTERY CHANGING INSTRUCTIONS

To replace battery remove this cover Replace battery with: either One type BA-5847 battery pack (plug connector into battery pack) or Four type BA-3030 D cells (Plug connector into internal socket)

5 THEORY OF OPERATION

5.1 General

This section presents a detailed description of the fuze and fuze setter system operation, with the intention of providing the design rationale for many of the circuits used. Various circuit functions are closely interrelated. Any circuit change contemplated must be examined for its effect on circuits not apparently related or for its effect at some time in the sequence other than the time under consideration. Some increase in circuit complexity is accepted to maintain fail-safe circuits, so that circuit failures will not cause an improper time setting, but will set the fuze to PD.

The M587 fuze and M36E1 fuze setter are fairly complex combinations of digital logic. To make it easier to follow the many signal paths it will be necessary to agree upon certain definitions and terms.

Initially, it is important to remember that both fuze and fuze setter have some similar functional areas, and that these must be kept separate in the reader's mind. For example, there is a fuze setter oscillator (frequency 2.4575 MHz + 0.005 percent) and a fuze oscillator (nominal frequency 10.24 kHz); there is a fuze counter (a 12-bit binary counter) and also a fuze scalar (a 9-bit binary counter).

The fuze setter communicates with the fuze during the setting operation by signals transmitted or received via the monitor line. Contact to this line in the fuze is made through the probe contact at the middle ring on the fuze nose. The fuze setter communicates with the fuze by causing the voltage on the monitor line to assume any of four voltage levels, which are identified herein as NEGATIVE, LOW, HIGH, and POSITIVE in order of increasing voltage. By switching between these states, signal paths between fuze clock and fuze counter and scalar are altered, and the states of individual MNOS memory devices are altered.

The LOW voltage state is a voltage near $-V_{DD}$ (approx. -25 V). When the monitor line is LOW, the fuze clock is disconnected from the fuze scalar and fuze counter.

The HIGH voltage state is a voltage near ground. When the monitor line is HIGH, the fuze clock is connected by fuze gating circuits directly to both the fuze scalar and fuze counter.

The POSITIVE voltage state is a voltage about +30 V. When the monitor line is POSITIVE, a positive polarizing voltage is applied to the gates of all the MNOS memory devices in the fuze counter, which results in the fuze counter initializing at a count of 3838 whenever fuze power is applied.

The NEGATIVE voltage stage is a voltage about -30 V. When the monitor line is NEGATIVE, a negative polarizing voltage is applied to the gates of all the MNOS memory devices in the fuze counter, which results, when the fuze power is next applied, in the fuze counter initializing at a count equal to the complement of the count in the counter at the time the monitor line was driven NEGATIVE. This is true for all counter stages except for the output stage M11, which initializes to 0.

To clarify the operation of the fuze setter, a functional description of the fuze electronics, shown in the block diagram of figure 13, is given before that of the fuze setter.

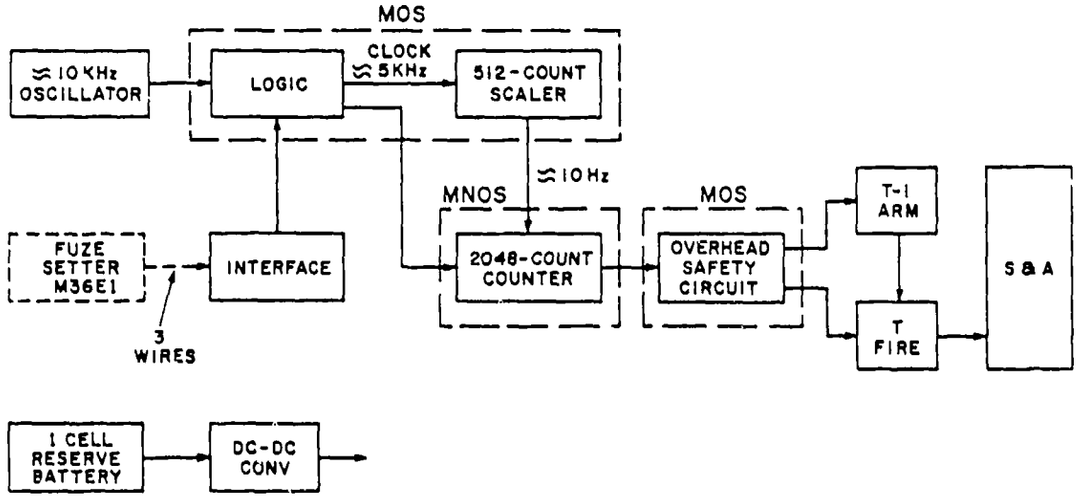


Figure 13. Block diagram of M587E2/M724 fuzes.

5.2 Fuze Functional Operation

In the fuze, the oscillator drives the logic circuit. The interface circuit, which is connected to the fuze setter, controls the gating of the oscillator to the scalar and the counter. When the monitor line between fuze and fuze setter is LOW (-25 V), fuze clock pulses of half-fuze-oscillator frequency are imposed on the monitor line, driving it about 1 to 5 V higher for half the period. No fuze clock pulses are sent to the scalar or counter. When the monitor line is HIGH (GND), both fuze scalar and fuze counter are driven by the clock pulses. These clock pulses also appear on the monitor line, driving it about 1 to 5 V lower for either half the period, or one quarter of the period, or not at all, depending upon the state of the fuze scalar and fuze counter.

The interface circuit also connects directly with the MNOS gate in the counter. A POSITIVE polarizing voltage on the monitor line is switched directly to the gates. A NEGATIVE polarizing voltage on the monitor line greater in magnitude than V_{DD} is also switched directly to the gates. The circuits described above are used during the setting operation.

In a normal timing operation after the gun is fired, no connection is made to the interface circuit from an external circuit. The dc-to-dc converter powers the system and causes the fuze clock pulses to drive only the scalar. The scalar, in turn, drives the counter in normal mode (10 Hz). The overhead safety circuit prevents the firing capacitor from charging before the arming signals occur. The arming signals occur at 0.2 and 3.4 s before set time. The 0.2 s arming signal is used only for set times $\leq$ 3.4 s.

5.3 Fuze Setter Functional Operation

The fuze setter nas a crystal-controlled 2.4576 MHz oscillator. The interface circuit connects with the fuze through three wires: ground, V_X for power, and the monitor line. The V_X connection is the third connection to be made to the fuze. When this connection is made, a resistor in the fuze interface circuit is connected between V_X and ground of the fuze setter. The fuze setter battery is connected to the power turn-on circuit in the fuze setter through the MODE switch. After a short time delay in this power turn-on circuit, power is applied to the dc-to-dc converter, energizing all fuze setter circuits. A reset circuit resets the logic circuits to their initial states, and the fuze setter counter starts counting 51.2 kHz fuze clock pulses.

The microprocessor controls all logic operations including reading the counter outputs, switching the interface circuit, and verifying all timing operations. The synchronism check assures that the fuze logic, fuze scalar, and fuze counter circuits are working properly. The setting switches establish the time to be set into the fuze. The display consists of light-emitting diodes that display the time set when the setting is correct. They display an E when the fuze does not set for any reason. They display a P when the fuze is set in the PD mode. Also, they indicate when the battery needs changing by presenting an L.

The battery is nominally 6 V. The dc-to-dc converter is used to provide the various positive and negative voltages required by the system.

During the setting operation, the fuze setter controls the fuze logic circuit and gates the fuze clock pulses to the fuze counter for 1/512 times the fuze time desired. The number of counts placed in the fuze counter depends upon the fuze oscillator frequency. The counts are stored in the fuze counter when the NEGATIVE polarizing voltage is applied to the MNOS transistor gates. Fuze oscillator calibration at the factory is not required.

5.4 Block Diagram Description

The fuze setter causes the sequence of events described above. The fuze setter electronics are block diagrammed in figure 14. The purpose of the various fuze setter blocks is described in the following paragraphs.

5.4.1 Power and Interface Circuit

The interface circuit switches the monitor line high and low, switches POSITIVE and NEGATIVE polarizing voltages to the monitor line, switches power to the fuze via the V_X line, and reads fuze clock pulses put on the monitor line by the fuze.

The interface circuit also senses the V_X contact and indicates when the V_X connection is making contact with the fuze. The fuze oscillator pulses, which are calibrated by the fuze setter, are received by the interface circuit and transmitted to the logic.

5.4.2 Power Turn-on Circuit

The power turn-on logic turns on the dc-to-dc converter, supplying system power, whenever the interface circuit senses a connection between the V_X contact of the fuze setter and the fuze. Power turn-on is delayed about 175 ms to eliminate multiple turn-ons caused by contact chatter between the fuze setter contacts and rings of the fuze nose. Power turn-off is delayed about 350 ms when the connection is broken. This insures that contact jitter during fuze setter removal will not reset and cause the fuze setter to cycle through only a partial setting operation.

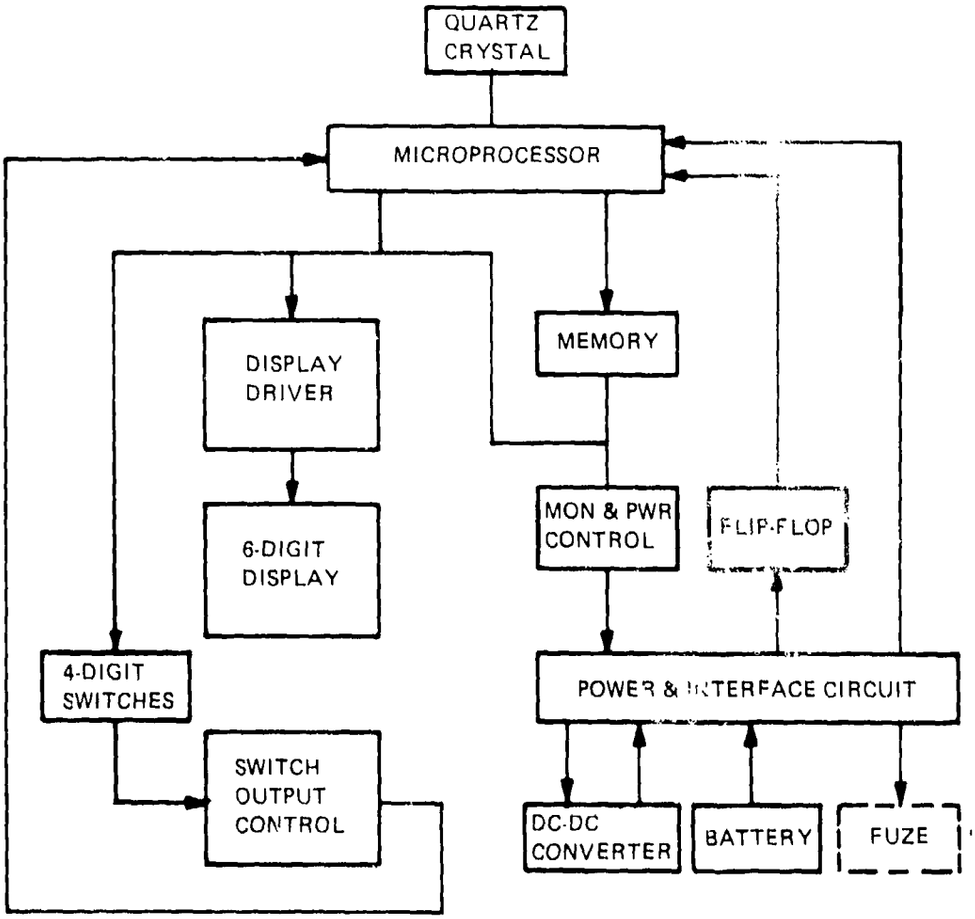


Figure 14. Fuze setter, block diagram.

5.4.3 DC-to-DC Converter

The dc-to-dc converter converts the 6 V battery to the various regulated voltages required by the fuze setter. The +30 and -30 V are employed in the interface circuit to generate the POSITIVE and NEGATIVE polarizing voltages and the V_X signal.

5.4.4 Battery

The battery supplies power to the entire fuze setter. The nominal battery voltage of 6 V is derived from one of three battery alternatives: a lithium battery pack, four alkaline D cells, or four zinc carbon D cells.

5.4.5 Monitor and Power Line Control

The monitor and power lie control provides the switching and holding logic circuits for switching the POSITIVE and NEGATIVE polarizing voltages on and off and for switching the monitor high and low voltages to the monitor line. It also contains circuits for switching and holding the V_X power on and off to the fuze.

5.4.6 2.4576 MHz Quartz Crystal Circuit

The 2.4576 MHz oscillator is a crystal-controlled oscillator circuit, which provides the precision time base for all circuits within the fuze setter. It is also used to calibrate the fuze oscillator during the setting cycle.

5.4.7 Display Driver and 6 Digit Display

The display driver is controlled directly by the microprocessor. The microprocessor supplies data which corresponds with the digits to be displayed by the light-emitting diodes (LED's). This information is stored in the display driver. On command, the clock in the display driver starts and, in sequence, displays the data on one 8 segment display at a time. The rate at which the display driver sequences through the displays gives the impression that they are all on at once.

5.4.8 4 Digit Switches

The mode switch allows an operator to apply power to the fuze setter and select the desired mode of operation. The operator may choose to either set a fuze time of between 000.2 to 199.9 s using the "0" or "1" position, set a fuze to the point detonation function (PD), or interrogate a fuze to discover its set time without changing its setting ("?").

The 3 digit setting switches allow the operator to select times from 000.2 to 199.9 s, They receive signals from the microprocessor, which then decodes the data to determine mode and time settings.

5.4.9 Switch Output Control

The switch output control is a parallel/serial shift register which receives the data which comes through the switches. These data are loaded into the shift register in parallel and shifted out to the microprocessor in serial form. The microprocessor then decodes the data to determine what the switch setting is.

5.4.10 Microprocessor

The microprocessor operates by following a predetermined program which is stored in the memory.

The microprocessor sends data through the switches via bus lines 0 through 5. These data are loaded into a shift register which returns through the switches to the microprocessor. The microprocessor then decodes the data and begins operation of the interface circuit. The microprocessor monitors the fuze clock through a flip-flop which reconstructs the clock for the microprocessor from leading and trailing edges.

The microprocessor also monitors the battery low circuit which indicates when the battery voltage drops to a level where fuze setter operation will soon end.

All timing and delay functions are performed by the microprocessor using timing loops. These loops are made up of a known number of program steps and each program step lasts a known amount of time. By counting the number of steps, one can control the time for an operation.

5.4.11 Memory

The memory contains 1024 bits of information organized into 8 bit "words." Each word is recognizable to the microprocessor as a command. A clock output from the microprocessor causes the memory to move through the stored "words" one at a time. The microprocessor moves through the words in memory in different ways. The different paths are determined by conditions such as the mode selected, the time selected, fuze errors, and battery condition. The memory also contains programming which causes the microprocessor to check itself and the memory.

5.4.12 Flip-Flop

The flip-flop is used to reconstruct the clock for the microprocessor. The interface circuit detects the leading and trailing edges of the fuze clock pulses. These edges are used to set and reset the flip-flop which recreates the fuze clock pulse. The flip-flop is also used to latch the turn-on pulses and battery low pulses from the interface circuit.

6. DETAILED DESCRIPTION

6.1 Interface Circuit

The interface circuit which is shown on the fuze setter diagrams figures 14 and 15 consists of discrete components that provide five basic functions:

(a) Sense the V_X contact to turn on the fuze setter.
(b) Convert the logic signal to the voltage that powers the fuze.
(c) Convert the logic signals to the appropriate monitor line voltages.
(d) Sense the fuze clock pulses on the monitor line.
(e) Sense the V_X contact for any discontinuity during the cycle.

The V_X contact, pin A of the fuze connector J1, is wired to terminal E1 of the power and interface board assembly A2. When the fuze setter is placed onto the nose of a fuze, an impedance of 3300 ohms with respect to 0 V is sensed. This impedance causes Q5 to saturate via CR6 and R4, which in turn causes Q1 to saturate via R2, R3 and R5. The $\overline{\text{TURN-ON IN}}$ signal at J1-8 of the power and interface board assembly A2, therefore, switches from 0 to -6 V. This signal is applied to the power turn-on logic.

When the $\overline{V}_Y$ signal is received from the monitor and power line control, connector J1-17 of the power and interface board assembly A2 switches from 0 to -6 V. This causes Q15 to saturate via R25, which in turn causes Q17 to saturate via R27 and R31, providing -30 V at the emitter of Q16. The 3300-ohm fuze impedance with respect to 0 V at the V_X contact causes Q16 to saturate via CR8, R11, CR1, and CR2. This applies approximately -27 V to the V_X line of the fuze via Q17, Q16, CR1, CR2, and CR8. This voltage is derived from the -30 V at the emitter of Q17 and the voltage drops through CR1, CR2, CR8 and the base emitter drop of Q16.

This saturation of Q16 also causes Q4 to saturate via R10. Resistor R7, which has an impedance of 3300 ohms with respect to 0 V via Q4, maintains Q1 in a saturated state via R3 and R5. The Q4 circuit is required when voltage is applied to the V_X line. This voltage cuts off Q5. It would appear as if a fuze disconnect had occurred if the Q4 circuit was not included. As long as the fuze setter remains in contact with the fuze, Q16 and Q4 remain saturated and no fuze disconnect signal occurs.

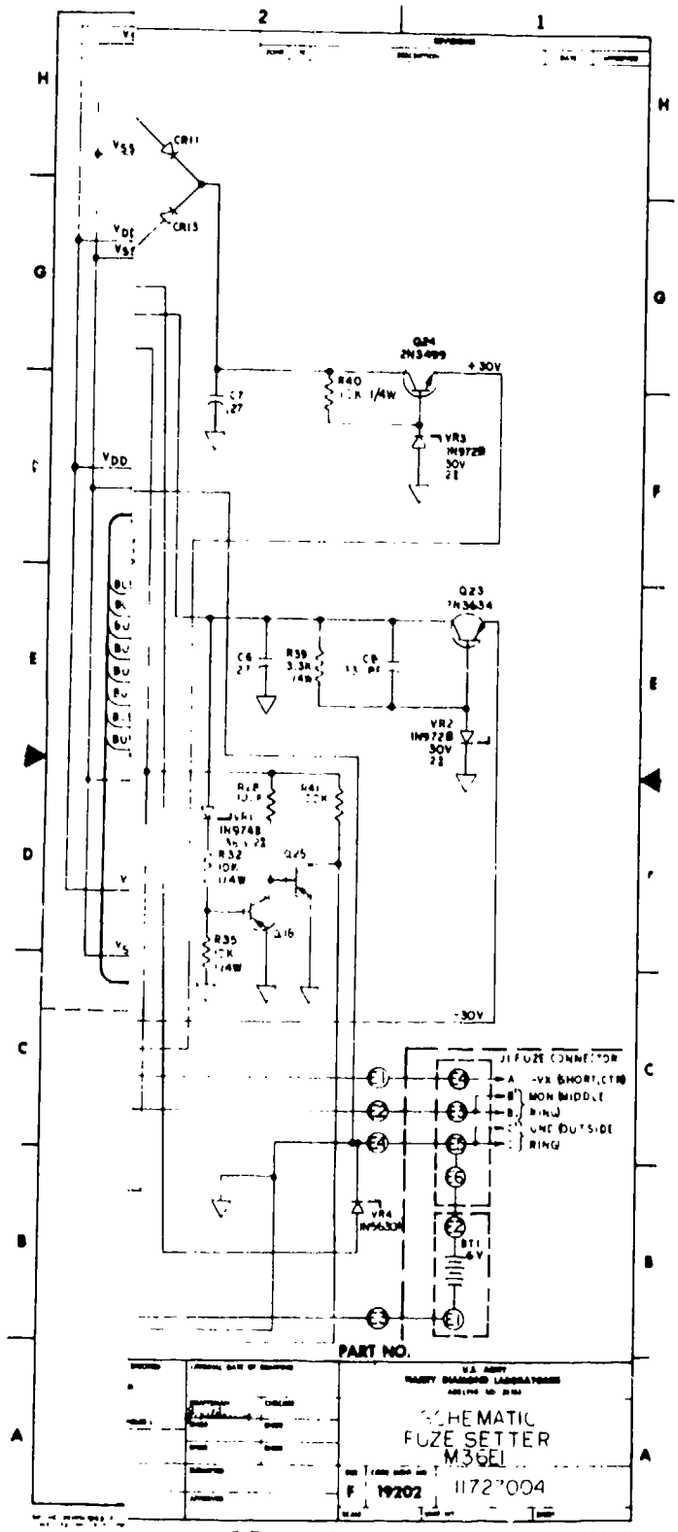
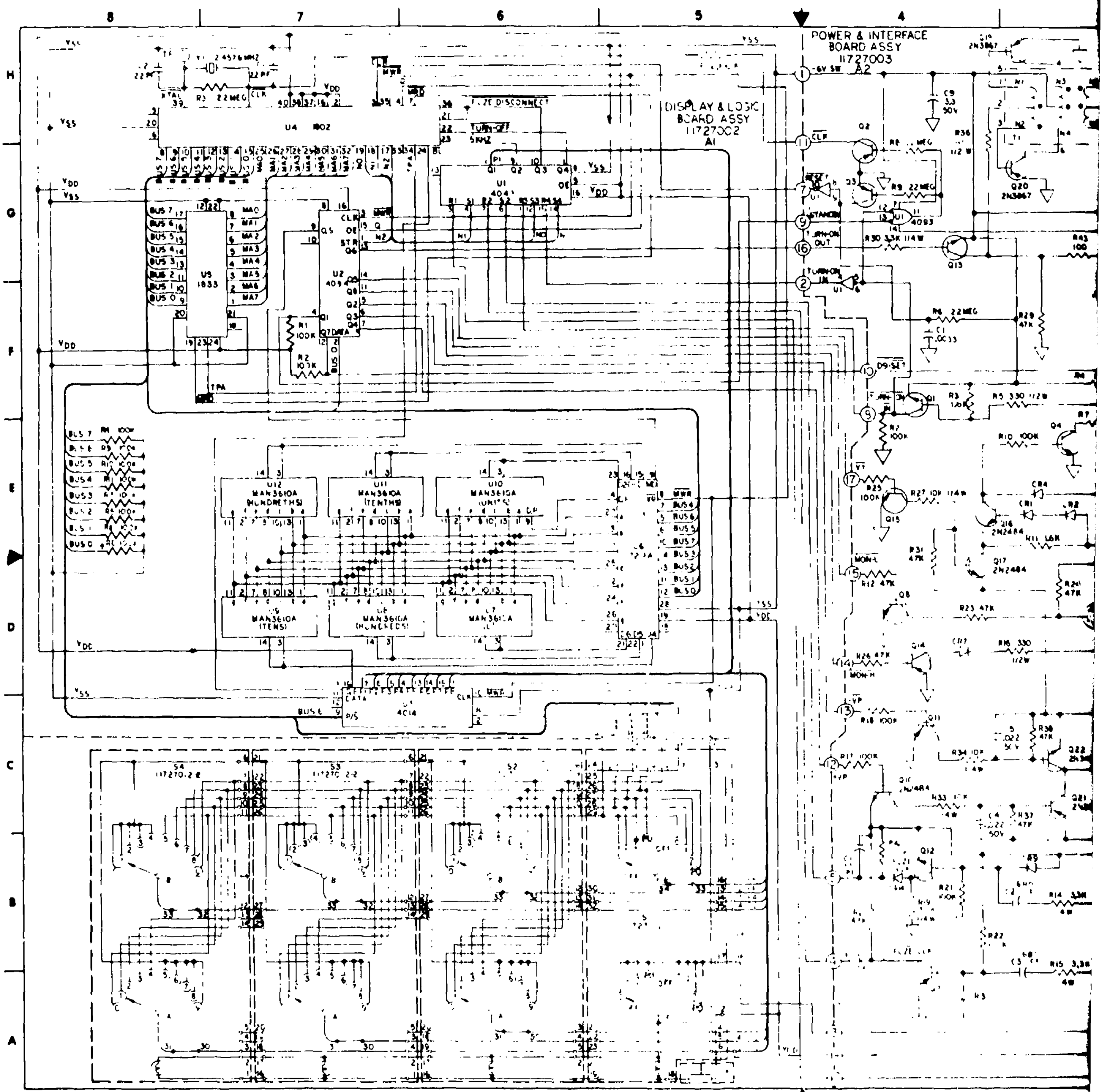


Figure 15. Fuze setter M36E1, schematic diagram.


POWER & INTERFACE
BOARD ASSY
11727003
A2
DISPLAY & LOGIC
BOARD ASSY
11727002
A1
U4 1802
U5 1833
U12 MAN3610A (HUNDRETHS)
U11 MAN3610A (TENTHS)
U10 MAN3610A (UNITS)
MAN3610A (TENS)
MAN3610A (HUNDREDS)
FUZE DISCONNECT
TURN-OFF
5MHZ
2.4576MHZ
8
7
6
5
4
H
G
F
E
D
C
B
A

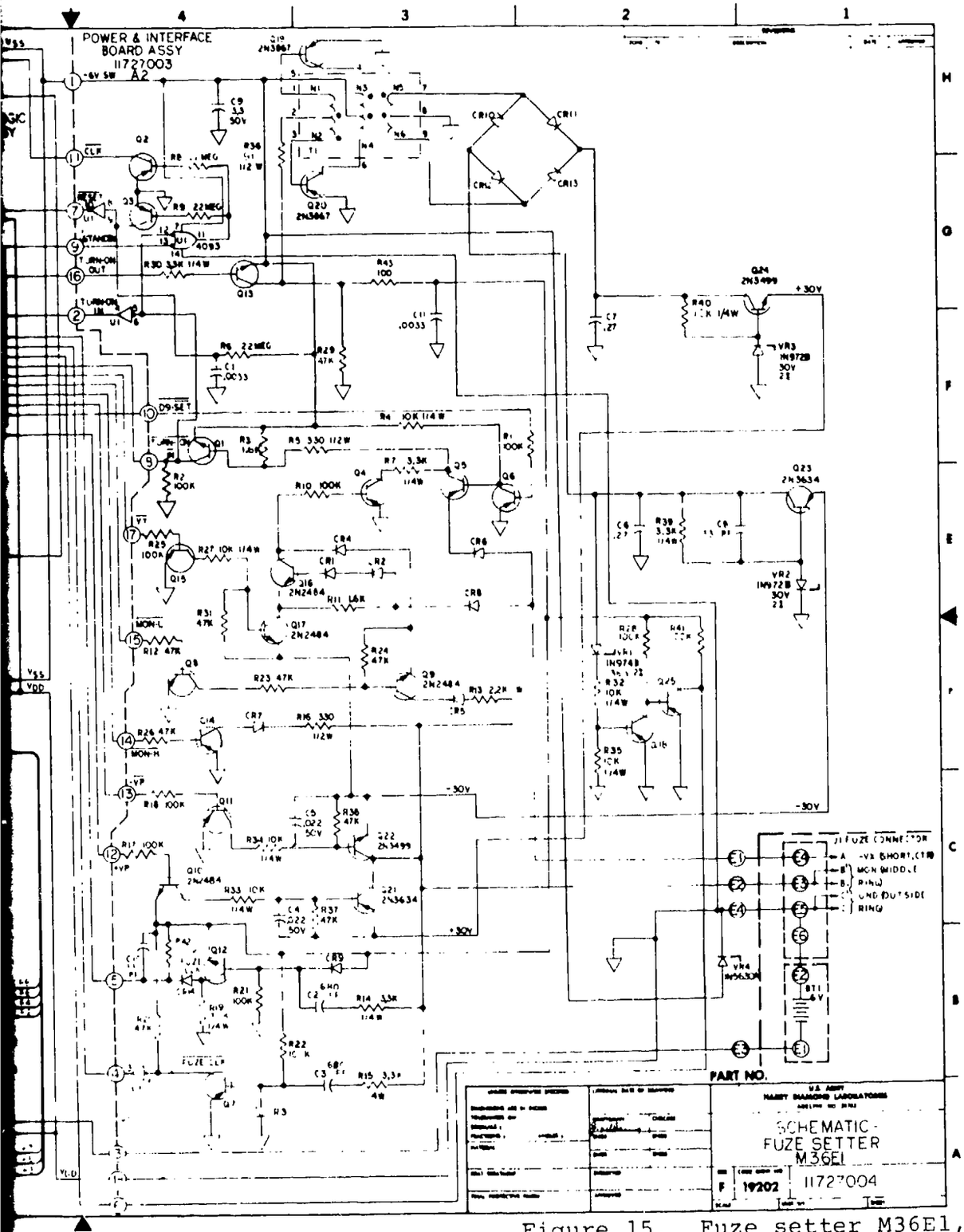


Figure 15. Fuze setter M36E1, schematic diagram.

Following the setting cycle, all power is removed from the V_X line for approximately 8 ms. This is accomplished by deasserting $\overline{V_y}$ to remove the connection to -30 V and by asserting $\overline{D9.\overline{SET}}$ to remove the connection to -6V.

The $\overline{D9.\overline{SET}}$ signal is sent from the serial/parallel shift register U2 to J1-10 of the power and interface board assembly A2. When this signal switches from 0 to -6 V it causes Q6 to saturate via R1, which in turn causes Q5 to cut off.

The monitor contacts, pin B and B^1 of the fuze connector J1, are wired to E2 of the power and interface board assembly A2. The four different voltage levels of the monitor line (NEGATIVE, LOW, HIGH, and POSITIVE) are generated by the interface circuit.

When the $-\overline{V}_p$ signal is received from the monitor and power line control, J1-13 of the power and interface board assembly A2, switches from 0 to -6 V. This causes Q11 to saturate via R18, which in turn causes Q22 to saturate, via R34, C5 and R38, thereby applying the NEGATIVE voltage to the monitor line.

When the $\overline{MON-L}$ signal is received from the monitor and power line control, J1-15 of the power and interface board assembly A2 switches from 0 to -6 V. This causes Q8 to saturate via R12. The monitor line is LOW only when power is applied to the fuze V_X line, which provides -30 V to the cathode of CR4. Therefore, when Q8 saturates, Q9 also saturates via R23 and R24, and applies the LOW voltage to the monitor line via CR5 and R13.

When the $\overline{MON-H}$ signal is received from the monitor and power line control, J1-14 of the power and interface board assembly A2 switches from 0 to -6 V. This causes Q14 to saturate via R26 and applies the HIGH voltage to the monitor line via CR7 and R16.

When the $+V_p$ signal is received from the monitor and power line control, J1-12 of the power and interface board assembly A2 switches from -6 to 0 V. This causes Q10 to saturate via R17, which in turn causes Q21 to saturate via R33, C4, and R37. The POSITIVE voltage is then applied to the monitor line.

When the fuze clock pulses are received on the monitor line they are converted to voltage levels suitable for the logic circuits by the interface circuit. Transistor Q12 is normally saturated via R21. When fuze clock pulses are present, each negative edge is differentiated by R14 and C2. This causes Q12 to cut off, which produces an output FUZE CLK pulse at J1-5 of the power and interface board assembly A2, employing R42 as a pull-down resistor. Diode CR9 is used to prevent any reverse bias on the base of Q12 due to the negative differentiated pulses.

Transistor Q7 is normally saturated via R22. When FUZE CLK pulses are present, each positive edge is differentiated by R15 and C3. This causes Q7 to cut off, which produces an output FUZE CLK pulse at J1-4 of the power and interface board assembly A2, employing R20 as a pull-down resistor and U1 as an inverter. Diode CR3 is used to prevent any reverse bias on the base of Q7 due to the positive differentiated pulses.

6.2 Power Turn-On Circuit

The input flip-flop receives a $\overline{\text{TURN}}$-$\overline{\text{ON}}$-$\overline{\text{IN}}$ signal at J1-8 of the display and logic board assembly A1, from the interface circuit, when a fuze connection is sensed at the V_x contact. After approximately 175 ms, the time allowed for contact "jitter," the TURN-ON OUT signal at J1-16 of the display and logic board assembly A1 is presented to the base of Q13 to turn on the dc-to-dc converter circuitry. When the fuze connection at the V_x contact is broken, the TURN-ON-IN signal is removed from the power turn-on logic. After approximately 350 ms, the time allowed to "break" the V_x connection to the fuze, the TURN-ON OUT signal is removed from the base of Q13 to turn off the dc-to-dc converter.

The power turn-on circuit consists of a power turn-on storage flip-flop, the microprocessor, and the interface control serial/parallel output register. The turn-on storage flip-flop receives two signals, the $\overline{\text{TURN}}$-$\overline{\text{ON}}$-$\overline{\text{IN}}$ signal at J1-8 of the display and logic board A1, and the TURN-ON-IN signal at J1-2 of the display and logic board A1. The TURN-ON-IN signal is held at -6 V by the output of inverter U1-4, whose input is held at 0 V

by pull-up resistor R2. When the fuze setter makes contact with the fuze, the TURN-ON-IN signal changes state from 0 to -6 V and the $\overline{\text{TURN-ON-IN}}$ signal changes state from -6 to 0 V. The fuze disconnect flip-flop (U1-Q3), which was previously set to a high (0 V) output by the microprocessor applying a 0 V pulse to the set input (S3), is unaffected by the $\overline{\text{TURN-ON-IN}}$ signal changing state from 0 to -6 V. If it changes state again from -6 to 0 V in the first 175 ms after initial contact, the flip-flop will reset and the $\overline{\text{FUZE DISCONNECT}}$ signal will switch from 0 V to -6 V The microprocessor will detect the change in state of the $\overline{\text{FUZE DISCONNECT}}$ line and start the 175 ms period over.

The change in state of the TURN-ON-IN signal initiates the microprocessor turn-on procedure. The TURN-ON-IN signal is applied to one input of a NAND gate (U1-12). The other input (U1-13) is held in a high state by the pull-up resistor R1 which is on the display and logic board A1. When the $\overline{\text{TURN-ON-IN}}$ signal changes state, so does the output of the NAND gate (U1-11). This causes transistors Q2 and Q3 to turn off. This immediately enables the crystal oscillator circuit by removing the high level at J1-11 of the display and logic assembly board A1. The reset signal at J1-7 of the display and logic assembly board also changes state, but it is delayed by approximately 50 ms. This delay is controlled by the time constant of the combination of R6 and C1. This delay allows the clock to reach proper frequency and amplitude before the microprocessor is enabled.

If constant contact is maintained for 175 ms, the microprocessor will enable the output of U2, the serial/parallel output register. This is accomplished when the microprocessor changes the state of the Q output line (U4-4) from -6 to 0 V. This signal is applied to the serial/parallel output register enable line (U2-15). This action presents the word stored in the output register to the power and interface board A2 input lines. The TURN-ON-OUT signal, which is one of these lines, changes state from -6 to 0 V. This turns on Q13 which supplies power to the interface circuitry and initiates the setting procedure.

If at any time after the initial 175 ms test period, the $\overline{\text{TURN-ON-IN}}$ signal changes state from -6 to 0 V, it will cause the $\overline{\text{FUZE DISCONNECT}}$ line to change states from 0 to -6 V. The microprocessor detects this change and causes the fuze setter to display an "E."

At the end of the setting cycle, the microprocessor sends a positive (0 V) pulse to the set line (U1-14) of the flip-flop that controls the $\overline{\text{TURN-OFF}}$ line. If there has been a loss of contact, the reset line of the flip-flop wil no longer be at 0 V and the pulse on the set line will cause the $\overline{\text{TURN-OFF}}$ line to change states from -6 to 0 V. The microprocessor checks for this change of states. The microprocessor will continue to send set line pulses until the $\overline{\text{TURN-OFF}}$ line changes states.

When the $\overline{\text{TURN-OFF}}$ line does change state from -6 to 0 V, the microprocessor starts a 350 ms checking routine to make sure that contact is not re-established. If contact is reestablished, the microprocessor starts looking for another loss of contact and starts the 350 ms checking routine again.

If there is no contact for 350 ms, the microprocessor puts the fuze setter back into a standby mode.

6.3 Dc-to-Dc Converter

The dc-to-dc converter is powered by the 6 V battery through the MODE switch. When the TURN-ON-OUT signal is received at J1-16 of the power and interface board assembly A2, the dc-to-dc converter supplies the two required voltages to the fuze setter circuitry. These voltages are +30 and -30 V.

The +30 V is employed to generate the POSITIVE polarizing pulse. The -30 V is employed to generate the NEGATIVE polarizing pulse and to power the fuze V_X line. It is also used to generate the LOW voltage on the monitor line.

When the TURN-ON-OUT signal is received at J1-16 of the power and interface board assembly A2, Q13 saturates via R30. The -6 V is then applied to the center-tap of the primary windings, N1 and N2, of T1 via R36. Resistor R29 is employed as a pull-up resistor to return the primary windings to 0 V when Q13 is cut off. Windings N1 and N2 in conjunction with windings N3 and N4 enable Q19 and Q20 to form the dc-to-dc converter oscillator. Capacitor C9 is employed as a filter. The T1 secondary windings N5 and N6 provide the "stepped-up" oscillator voltage.

A full-wave rectifier bridge is employed, consisting of CR10, CR11, CR12, and CR13, to provide the unregulated voltages of approximately $\pm$ 50 V. The +50 V is used to supply the +30 V regulator, consisting of C7, R40, VR3, and Q24. The -50 V is used to supply the -30 V regulator, consisting of C6, R39, C8, VR2, and Q23.

6.4 Battery

The battery powers all the circuits of the fuze setter. The battery voltage of approximately -6 V is provided by one of three battery alternatives: a lithium battery pack, four alkaline D cells, or four carbon-zinc D cells. The negative terminal of the battery is connected to the power and interface board assembly A2 via terminal E3. The positive terminal of the battery is connected to the power and interface board assembly A2 via terminal E4.

6.5 Low Voltage and Reset Circuit

The low voltage and reset circuit monitors the output of the dc-to-dc converter. Since the -50 V output of the dc-to-dc converter is proportional to the battery voltage, a voltage sensing circuit is employed to monitor the -50 V. When the -50 V decreases in magnitude to less than approxima ely 33 V, Q18 changes from saturated state to a cut-off state via VR1, R32, and R35. The BATT-LOW signal at J1-6 of the power and interface board assembly A2 will then switch from -6 to 0 V when Q25 saturates via R28 and R41. This indicates that the battery voltage has decreased in magnitude to less than approximately -4.5 V.

When the BATT-LOW signal changes states from -6 to 0 V it causes a flip-flop (U1-3) to reset, that is, change states from 0 to -6 V. This flip-flop output, signal P1 (U1-2), is loaded into one of the parallel inputs (U4-7) of the switch output control shift register. Twice during the program the microprocessor checks this bit of data, once in the beginning of the program and once before the display is energized. When checking this data bit, the microprocessor sends seven low pulses out on the MWR signal line. This causes the data from the P1 line (BATT-LOW signal) to be shifted out on the Q8 line (U3-3). When the BATT-LOW data bit is on the Q8 line it is read by the microprocessor on U4-24. If its level is low (-6 V) the first time it is checked, the microprocessor causes a display of "L" only and does not set the fuze. If a low level is detected on the second check, the microprocessor displays an "L," along with the normal setting display.

6.6 Monitor and Power Line Control

The monitor and power line control provides the appropriate signals to the interface circuits to control the fuze power supply V_x voltage and the voltage levels on the monitor line. This information is transmitted at the proper times by the microprocessor. All information transmitted originates in the microprocessor.

The monitor and power line control consists of a serial/parallel shift register, a microprocessor, and the memory. All signals for the interface and power board A2 are transmitted through the serial/parallel shift register (U2). The program in the memory contains all the required data words to create the different voltages and signals that are required to control the monitor line. These data are taken into the microprocessor, on the eight bus lines, at the proper time in the program. They are then shifted out of the microprocessor into the serial/parallel shift register on bus line 0 (U4-15). These data are stored in the internal latches of the shift register when U1-2 is strobed high by the microprocessor. At the proper time, the outputs of the shift register are enabled by applying a (0 V) positive pulse to the output enable line (U2-15). When the outputs are enabled, all the interface lines are simultaneously changed to the proper states for the current section of the setting cycle. The timing cycles in the microprocessor determine what time to make the changes in the interface circuits status.

The TURN-ON OUT line is controlled by U2-13. The application of a high level (0 V) on J1-16 of the power and interface board assembly A2 activates Q13 and supplies -6 V, +30 V, and -30 V to the interface circuit.

The D9-$\overline{\text{SET}}$ line is controlled by U2-12. Application of a low level (-6 V) to J1-10 of the power and interface board assembly enables Q6 and removes power from the V_X line to the fuze.

The $\overline{V_Y}$ line is controlled by U2-14. Application of a low level (-6 V) to J1-17 of the power and interface board assembly A2 enables Q15 and produces a -30 V level on the V_X line to the fuze.

The $\overline{\text{MON-L}}$ line is controlled by U2-11. Application of a low level (-6 V) to J1-15 of the power and interface board assembly A2 enables Q8 and produces a -25 V level on the monitor line to the fuze.

The $\overline{\text{MON-H}}$ line is controlled by U2-5. Application of a low level (-6 V) to J1-14 of the power and interface board assembly A2 enables Q14 and produces a 0 V level on the monitor line to the fuze.

The $-\overline{V_P}$ line is controlled by U2-6. Application of a low level (-6 V) to J1-13 of the power and interface board assembly A2, enables Q11 and produces a -30 V level on the monitor line to the fuze.

The $+V_P$ line is controlled by U2-7. Application of a high level (0 V) to J1-12 of the power and interface board assembly A2 enables Q10 and produces a +30 V level on the monitor line to the fuze.

6.7 2.4576 MHz Oscillator Circuit

The 2.4576 MHz oscillator provides the highly accurate time base for the fuze setter. This oscillator is crystal controlled and is employed to calibrate the fuze oscillator during the setting cycle.

The oscillator consists of two inputs to the microprocessor, U4-1 and U4-39, and crystal Y1 on the display of logic board assembly A1. Other associated components are R3, C1, and C2.

6.8 Display Driver and 6 Digit Display

The display driver provides in a single package all the circuitry necessary to interface the microprocessor to the 7 segment displays. Included on the chip is an 8x8 static memory array providing storage for the displayed information. A 7 segment decoder, the multiplex scan circuitry, and the high-power digit and segment drivers are also included in the package. A FET is used to apply power to the display driver after fuze contact. This circuit prevents display activation when the power is applied to the fuze setter logic circuitry.

The data to be displayed by the display driver are received via the bus lines on pins U6-5, 6, 7, 10, 11, 12, 13, and 14. Included in this information is the type of decoding to be used (CODE B), the operational mode (cycle or shutdown), and the data to be decoded. Pin U6-8 receives a $\overline{MWR}$ signal from the microprocessor (U4-35) that tells the display driver when to accept information. When pin U6-9 is in a high state, the display driver reads the eight data lines to find which mode of operation it is to work in. After the display driver receives the data to be displayed, it receives a new mode command which takes it out of the shutdown mode and starts the display. The output to the display is multiplexed. Power is supplied on lines U6-15, 16, 17, 21, 22, and 23. The display data are supplied in parallel on lines U6-1, 2, 3, 4, 24, 25, 26, and 27. For example, when U6-22 is energized, the data for the hundreds display digit are put on the eight data lines. Power would next move to U6-16 and data for the tenths display digit would be put on the eight data lines. The display driver moves through this random sequence at one digit every 500 μs. At this rate it appears that all the digits are illuminated at the same time.

6.9 Mode and Setting Switches

The mode switch is employed to apply power to the fuze setter and to select the desired mode of operation. The mode switch has 10 positions: two positions each of "OFF", "0", "1", "?", and "PD."

In both the "OFF" positions, no power is applied to any circuitry in the fuze setter. In the other positions, power is applied to all of the display and logic board assembly A1 and to the emitter of transistor Q13 on the power and interface board assembly A2.

In both the "0" positions, a fuze may be set to times between 000.2 and 99.9 s in 0.1 s increments.

In both the "1" positions, a fuze may be set to times between 100.0 and 199.9 s in 0.1 s increments.

In both the "PD" positions, the operator may set a fuze to the point detonation function.

In both the "?" positions, the operator may interrogate a fuze to find out to what time it has been set without changing its setting.

Each of the four setting switches is a 2 pole 10 position switch. The mode switch has one pole dedicated to powering the unit. Positions 2 through 5 and 7 through 10 apply power to the unit. Positions 1 and 6 are the off positions and no power is applied. The second pole is used to select the mode of operation.

The setting switches use both poles to determine what time has been set. On one pole, the first five positions are tied together and the last five are tied to the bus lines. On the second pole, the first five positions are tied to the bus lines and the last five positions are tied together.

The six poles from the setting switches and the one pole from the mode switch are tied into the parallel inputs (P2-P8) of U3, a parallel/serial shift register.

A data word is placed on the bus lines, which has seven bits set to a low level and one bit set to a high level. This word is connected in parallel to all the switch positions. If the switch is in a position that corresponds to the bus line with the high level, it will have a high level on its pole and this level will be loaded into the shift register. The data in the shift register are then serially loaded into the microprocessor (U4-24).

The microprocessor puts out six words, changing the bus line with the high level each time. After each word is output, the microprocessor checks the data in the shift register. The microprocessor can determine which bus line has the high level and which poles have the high levels. Using this information the microprocessor can determine the position each switch is in. The microprocessor can also determine whether a switch is open or shorted. If a pole has a high level on it for more than one word, it is shorted; if a pole never has a high level, it is open. If either of the above cases occurs, the fuze setter will display an "E" indicating an error.

6.10 Microprocessor and Memory

The microprocessor is a large-scale-integrated circuit/CMOS 8-bit, register oriented, central processing unit. The microprocessor includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in the memory.

The memory is a static 8192-bit mask programmable CMOS read-only memory organized as 1024 words by 8 bits and designed for use in microprocessor systems. The memory responds to a 16-bit address multiplexed on eight address lines. Address latches are provided on chip to store the eight most significant bits of the 16-bit address.

The memory contains a program, or sequence of control words, which when called to the microprocessor bus lines (U4-8 through U4-15) causes the microprocessor to perform various input, output, and timing functions.

When the $\overline{\text{TURN-ON-IN}}$ signal is activated by contact with a fuze, the crystal oscillator circuit is enabled and the microprocessor is taken out of the reset mode. The microprocessor then addresses the memory via the memory address lines (U4-25 through U4-32). The memory returns a control word to the microprocessor via the bus lines. This control word instructs the microprocessor to perform an operation. The microprocessor then addresses the memory again on the memory address lines, a new control word is sent to the microprocessor, and the operation is continued. In most cases a series of control words is needed to complete an operation.

Using this procedure the microprocessor can perform many different functions. In the fuze setter, the microprocessor is used for all timing functions, it controls all fuze interface functons, it monitors the battery voltage level, it monitors for

fuze contact, it supplies all data to the display driver, and it reads and checks the setting switches. A more detailed description of how these functions are carried out is included in the description of the software which follows in section 6.11.

6.11 Software Control Sequence

The following is a description of the program which is used to control the fuze setter. Each descriptive paragraph represents many command words and their overall effect. The addresses are not always in order because they follow the true flow of the program which jumps from place to place in the memory. Some instructions are referred to by name (i.e., "SEDIS"). These instructions in most cases represent a complete subroutine in the program and are referred to in order to simplify the explanation. In some cases "registers" are referred to. These are word storage areas in the microprocessor.

6.11.1 Start Up

Power is applied to the fuze setter by setting the mode switch to the desired position. The fuze setter is then placed over the fuze and upon contact, a 175 ms delay is initiated within the fuze setter. If there is a contact break between the fuze setter and the fuze, the 175 ms delay is restarted.

At contact, the $\overline{\text{TURN}}$-$\overline{\text{ON}}$-$\overline{\text{IN}}$ signal changes state from 0 to -6 V. Fifty ms after contact, the fuze setter enables the clock and releases the microprocessor reset state. This enables it to start operating at its reference time zero.

The microprocessor monitors the next 125 ms before applying fuze setter power to the fuze. It is during this time that the microprocessor performs a self test and presets certain registers to point to subroutines that are required for the remainder of the program.

The self-test program is part of the initial delay. The program sequence is as follows:

Data are set in the accumulator.
The "SEP 15" instruction transfers the data (least significant bit first) to the data register IC (U2).
The "OUT 7" instruction latches the data in the IC and sets the microprocessor EF2 and EF3 lines.
The "STR 9" instruction enables the serial output of the register that disables the display chip.

The "SEQ" instruction enables the register output which applies power to the power and interface circuits via the TURN-ON OUT signal. This output enable will be in effect until it is reset at the end of the program.

6.11.2 Self-Test Program

The self-test program loads and recalls all registers except those required to point to subroutines required for display.

A one is added to the data word called from the last register. If a carry results, the self-test continues (indicating no lost bits); if not, the program defaults to the error routine and displays the character "E."

A pseudoprogram is exercised to test the most often used instructions with a continuous test for errors. If an error occurs, the program defaults to the error routine.

A sum check is started and proceeds by adding the hex contents of ROM (U5) to the accumulator. The arithmetic overflow is ignored and only the accumulator bits are of importance. After each addition, the address is decremented by one and the addition is repeated. The process is repeated until the addition at address 0000 HEX. The final sum is then subtracted from a predetermined number which is determined by the contents of the memory and should result in the accumulator containing 00 HEX.

If no bits are lost in ROM U5, the above result is true and the program returns to the main body and continues in normal sequence. If the result is not true, the program defaults to the error routine to display an "E."

6.11.3 Battery Low Test

The battery low latch is cleared with an "OUT 2" instruction before the test of the battery low state. If the battery is not low, the program continues on to testing of switches; if the battery is low, the program branches to display character "L."

6.11.4 Test Mode Switch

All four mode positions are tested for switch closure. Each time a closure is found, register 3 is incremented by one. After the fourth switch position is tested, register 3

is tested for one. A number larger or smaller than one will cause the program to default to the not-set routine (error).

If closure was detected in the first position ("0"), the program will continue to test the remaining switches after register 3 is incremented.

If the second position ("1") is selected, a binary equivalent to 100 is loaded into register 9. Register 9 will contain a final value equivalent to the number set on the switches. The program will then continue to test the remaining mode switch positions.

In the third position ("?"), if switch closure is detected, the mode flag (register 3) is incremented by one and the interrogate flag (? Flag) is set.

In the fourth position (PD) if closure is detected, the P flag is set.

If not in PD mode, register 3 is tested for a one. If the register is not a one, the program branches to the not-set routine. If it is a one, the program continues in fuze set routine.

6.11.5 Test Switch Data

A binary weighted table is pointed to by register 12. The sum routine address is located in register 2.

Register 8 contains the number 3 to keep track of which switch is under test.

Register 7 holds the number of shifts required to reach the bit to be tested.

Register 13 starts with the number for two passes per switch.

Register 10 is set to zero and will count the number of positions tested until the switch closure is found.

The switch test, which follows, will be repeated twice for each of the three switches tested.

Test word 41HEX is located in high register 5. The 1 of 41HEX is the test bit and will be the bit shifted as each switch position is tested. The 4 of 41HEX is the parallel enable bit for the static shift register (U3).

Low register 5 contains the number 5 equal to the five switch positions to be tested in each of the two passes per switch (positions 0 to 4 and 5 to 9).

The number of shifts is copied into work register 4. The original number is preserved in register 7.

Data are output to the switches and latched in the static shift register (U3).

The data in the static shift register are shifted one place to the left.

Register 4 is decremented if it is not zero. The data in the X static shift register are shifted one more place to the left.

The $\overline{EF1}$ (U4-24) flag is tested for switch closure.

If closure is present, the program branches to subroutine "Sum 9" to sum up the value of the switch position. If no closure is present, the program increments the number of switch positions tested, decrements the number of switch positions to be tested, and tests for zero.

If there are more switches to be tested, the switch test data are shifted one bit to test the next switch position. At this time, the program jumps back and repeats the loop.

When there are no more switch positions to be tested, the program increments the shift count number and decrements the two passes per switch count. If this count is not zero, the loop is repeated.

If the count is zero, the program decrements register 11, which stored the number of times that the "Sum 9" routine was entered. If register 11 is not zero, the program branches to the error routine. If it is zero, the subroutine "BNWHT" table address is incremented by two.

Also, if register 11 is zero, register 9 (switch data) is copied into register 12 (backup register) and the program tests for the minimum allowable time set. If this time is less than the minimum, the program branches to the error routine. Otherwise, the data are set into the fuze.

6.11.6 Sum 9 Routine

The number of times this routine is used for each switch is stored.

When the switch position number is zero, this routine exits and the main program continues.

The program takes the number from the "BNWHT" table and adds to register 9 (switch setting, converted to a binary number).

The program decrements the switch position number and repeats the loop.

6.11.7 PD Mode

During the mode test, if the PD mode is selected, the program branches to this routine to test the mode flag for multiple switch closures and to set the P flag. The program then continues to the setting routine.

6.11.8 Fuze Set Preliminary

At the beginning of this routine, the monitor line is set POSITIVE for 50 ms to preset the fuze counter to receive the new set time.

The monitor line is then set high for 10 ms and the D9.$\overline{\text{SET}}$ line is set low. This will cut off the voltage to $-V_X$ (fuze power line).

The program tests for fuze disconnect.

The monitor line is first set low and then power is applied to the fuze.

The D9.$\overline{\text{SET}}$ line is set high.

The interrupt latch (U1-11) is reset before the microprocessor's internal interrupt is enabled.

The next instruction will cause the monitor line to be set into the high state immediately after the last quarter-width pulse is detected as described below.

The fuze clock is checked for accuracy by testing the pulse-width of each pulse in a series of pulses with the pulse width routine. The pulses are half-width pulses and quarter-width pulses with respect to the fuze oscillator period.

At the conclusion of the fuze pulse train, there is a delay before the fuze sends its last quarter-width pulse. If this pulse is not detected after the proper delay time, the program branches to the not-set routine.

6.11.9 Set Fuze Time

The PD flag is tested and if it is set, the program branches to the not-set routine to set the fuze to the point detonation mode.

The switch time is set into the fuze by counting down the number stored in register 9. The time set is terminated at the end of the countdown by setting the monitor line low.

6.11.10 Interrogate fuze

This section of the program can be entered from three different points in the program.

When the "?" mode has been selected, the entry is made from the switch mode routine.

This routine is also a normal continuation of the fuze-set mode and is used to test the accuracy of the new time set in the fuze.

In the PD mode, entry will be from the PD portion of the not-set routine to test that PD has been set into the fuze.

In this section of the program, the three modes share many common instructions and those instructions not applicable to the interrogate or PD modes are jumped over by branch instructions.

For clarity, this section will be split into two sections. The first describes the SET/PD time check modes, and the second (paragraph 6.11.11) describes the interrogate mode.

The monitor line is set low to disconnect the fuze clock from fuze scalar and fuze counter. This state is held for 2 ms in the fuze set mode only.

The monitor line is then set negative. This NEGATIVE polarizing voltage is applied to the memory of the fuze counter and will cause the count in the fuze counter to be complemented when fuze power is next applied.

The NEGATIVE polarizing voltage is held for 50 ms.

The monitor line is set low and D9.$\overline{\text{SET}}$ is set low for 2 ms. This removes all voltage from the V_X line, assuring that the fuze clock is turned off.

The monitor line is then set high. The fuze setter interrupt line is disabled and power is removed from the fuze for 8 ms.

The monitor line is set low. The fuze clock is disconnected from the fuze scalar and fuze counter.

Power is then reapplied to the fuze. The fuze setter interrupt line is enabled and D9.SET is reset to a high state. This condition is maintained for 10 ms.

Then the monitor line is set high. The pulse-detect routine is completed and the fuze clock is reconnected to the fuze counter and scaler. The prescaled count is now readied for countdown to test the fuze count.

The program tests the monitor line for a pulse. If a pulse occurs at this time, the number set into the fuze counter is too small.

The test for a pulse on the monitor line is continued. A pulse must be present before the count in register 7 is counted down to zero for the fuze set time to be within tolerance. If the count is out of tolerance, the program branches to the not-set routine.

The fuze set and verification routine ends here. The fuze setter interrupt line is disabled at this point.

6.11.11 Interrogate Mode Fuze Test

The monitor line is set low. The fuze clock is disconnected from the fuze scalar and fuze counter for 2 ms. After an additional 50 ms, the D9.$\overline{\text{SET}}$ is set low, removing all voltage from the fuze $-V_X$ lines.

Fuze power is then turned back on. The D9.SET line is reset high, allowing power to be applied to the $-V_X$ line.

The fuze interrupt is enabled followed by a 10 ms. delay.

In the interrogate mode, the data are transferred from register 12 to register 9 to maintain correct timing.

The detect routine is started to find the fuze output pulse. It must occur within a 0.1 ms window. The monitor line is then set high and the fuze clock is applied to the fuze scalar and counter.

A test number is preset before counting the time in the fuze. This preset number takes into account the time required for the minimum set test.

The program loads the number used for the PD count test.

The monitor line is tested for the coincidence pulse. If the pulse occurs before the test number is decremented to zero, the fuze is set in the PD mode.

When the test number count is at zero and the fuze is not in the PD mode, the "?" flag is tested. If this flag is not set, the program branches to the error mode.

The fuze set time is counted starting here.

To obtain the time set into the fuze, the elapsed time between the detect pulse and the coincidence pulse is measured by counting up a binary number.

This loop test for the coincidence pulse stores the count and tests that the binary count does not exceed the maximum allowable time set.

Because of the structure of the loop, when the coincidence pulse is detected, the program branches to adjust the count according to where the pulse detection takes place. The adjustment can be one, two, or three increments.

If the count exceeds the maximum allowable number, the program branches to the error routine. If not, the interrupt line (U4-36) is disabled.

The static shift register (U3) is set up at this point in the program for a battery low test.

Data representing a "blank" are loaded into the registers used for the four least significant display locations.

The battery low line (U1-2) is tested and data representing "L" or "blank" are stored in the register.

Fuze power is then turned off.

Error flags are tested for and then branches to the display routine.

The data word for "P" is loaded into the register and the "P" flag is tested. If the flag is set, the program branches to the display routine. If it is not set, the "P" data word will subsequently be replaced by appropriate data.

The binary number representing the set time must be displayed in a decimal form. A check is made to test that the binary number is greater than the minimum permissible number.

6.11.12 Binary to BCD Conversion

The binary number is converted to a decimal equivalent with 19999 (199.99 s) being the largest possible number and 20 (0.20 s) being the smallest. The leading zeros are blanked and a decimal point added behind the units digit.

First a binary equivalent equal to 10000 is subtracted from the number. If the stored number is the larger number, a one is loaded into the appropriate register. If the stored number is the smaller number, 10000 is then added back to restore the original number.

This process is repeated with the number 1000 being subtracted. With each subtraction, the appropriate register is incremented. When the stored number is smaller than 1000, 1000 is then added back; thus, the tens count is established.

The units count and the tenths count are decoded with the same procedure. After the tenths number is decoded, the remaining number is the hundredths number.

The interrogate "?" flag is then tested. If it is not set, the hundredths character is blanked.

The display driver IC is then engaged, the output code for data coming, followed by the display character data (eight characters), is sent. Lastly, the run display code is sent. Information for eight characters is output, but only six will be used.

6.11.13 Run Display Routine

The delay flag is set and the counts for the 5 s delay and 350 ms delays are entered.

Once the display is on and the delay flag is set, the 5 s delay is counted down. With each decrement, the fuze disconnect flag (U4-22) is tested. As long as there is no fuze disconnect, this loop is repeated until the 5 s delay has elapsed. At this time the delay flag is reset and the display is turned off. After the 5 s delay has elapsed, the program continues to look for a fuze disconnect, and when it is found, the 350 ms delay starts to count down. As long as the fuze disconnect continues, the 350 ms delay will count to zero. If contact is made before the 350 ms delay is over, the program looks for another disconnect which initiates another 350 ms delay.

At the end of the 350 ms, if no contact is made, the fuze interface is disabled and the program ends.

If a fuze disconnect occurs during the 5 s delay, the 350 ms delay is started and is decremented along with the 5 s delay. At the end of the 350 ms delay, the display is turned off, the fuze interface is disabled, and the program ends.

If the 5 s delay should count to zero before the 350 ms delay reaches zero, the display is turned off and the 350 ms delay continues to its end before the fuze interface is disabled and the program ends.

6.11.14 Error/PD Routine

The error routine is initiated at this point by an external interrupt on the fuze disconnect line (U4-36) or by the "Sep 1" instruction whenever a failure occurs in the execution of the program.

The display data for the character "F" are loaded.

The monitor line is set high at this time and the fuze power is removed. External microprocessor interrupt is disabled.

If the ? flag is not set, the monitor line is set positive for 50 ms. This will set the fuze counter for point detonation in the PD mode if an error is detected in the set mode.

If the interrogate flag was set, a test is made to see whether error data are present in the display register. If the program is in the set mode, an immediate branch is made to the display routine; if not, a branch is made to the interrogate routine to set the PD count and to test the set time.

6.11.15 Pulse Detect Routine

A number is loaded into registers 4 and 5. This number is the number of times the loop will be repeated while looking for the leading and trailing edges of a pulse. Register 4 is the working register and is decremented till each edge is found. Register 5 is used to restore the original number back into register 4 after each edge has been found.

The program tests for a positive-going edge of a pulse. If the pulse fails to appear, the error routine is called.

The program tests for a negative-going edge of the pulse. If the pulse fails to go negative, the error routine is called.

The monitor line high is set high with the "OUT 4" instruction.

6.11.16 "Sum 9" - Transpose Switch Position to Binary Weighted Equivalent

Register 11 is incremented by one each time this routine is entered. Only one entry per switch is permitted.

The switch position number is tested, and if it is zero, this program branches back to the main program.

Each switch is weighted by a binary equivalent to 16 bits. For example, the 10's switch binary equivalent is 03E8H (1000 decimal). The switch sum is stored in register 9.

After each switch position is summed, the switch position register is decremented and tested for zero.

In the main program, this routine is checked to assure that it was entered only once for each switch. If it was not entered, the switch has open contacts, and if it is entered more than once, the switch has shorted contacts.

7. CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The following conclusions are derived from the tasks performed during this program:

(a) The 13 fuze setters, S/N 1001 through 1003 and 1006 through 1015, which were subjected to the environmental test program, show that the design will withstand the environments normally encountered in field use.

(b) The reliability analysis indicates that the MTBF for the fuze setter is 64,000 hours and, therefore, there is a high level of confidence that this device will perform very successfully.

(c) The safety analysis of the fuze setter shows that the probability of improperly setting a time into a fuze is 3.0×10^{-9}. This makes the fuze setter acceptable for field usage.

(d) Use of microprocessor circuitry has increased the reliability, maintainability, safety, and portability of the fuze setter.

(e) The M36E1 fuze setter's smaller size and lower weight makes it easier to use in a field situation.

(f) The fuze setter probe design will provide self-alignment when interfaced with a fuze and guarantees proper connection with the fuze setting rings.

(g) The performance characteristics of the fuze setter battery enables the fuze setter to be operated and stored over wide temperature extremes.

7.2 Recommendations

The following suggestions are recommended to aid in the fabrication of production quantities of the fuze setter for use in the field.

(a) Fabricate, test, and deliver an initial production quantity of fuze setters in accordance with the technical data package to show feasibility of large production quantities.

(b) Review the fuze setter assembly and manufacturing procedures from a production engineering standpoint to provide a more cost-effective unit for large production quantities.

(c) Initiate a study to determine the requirements for the design and development of production test equipment for the fuze setter which would aid in minimizing the production costs for the fuze setter.

The enactment of these suggestions will further enhance the fuze setter system, providing a more suitable product for artillery field employment.

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